AXIOMTEK

CEM842/843

Intel® Celeron® J1900/N2807
Intel® Atom™ E3845 COM Express™
Type 6 Compact Module

User's Manual

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CAUTION

If you replace wrong batteries, it causes the danger of explosion. It is recommended by the manufacturer that you follow the manufacturer's instructions to only replace the same or equivalent type of battery, and dispose of used ones.

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ESD Precautions

Computer boards have integrated circuits sensitive to static electricity. To prevent chipsets from electrostatic discharge damage, please take care of the following jobs with precautions:

- Do not remove modules or integrated circuits from their anti-static packaging until you are ready to install them.
- Before holding the module or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. It discharges static electricity from your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling modules and components.

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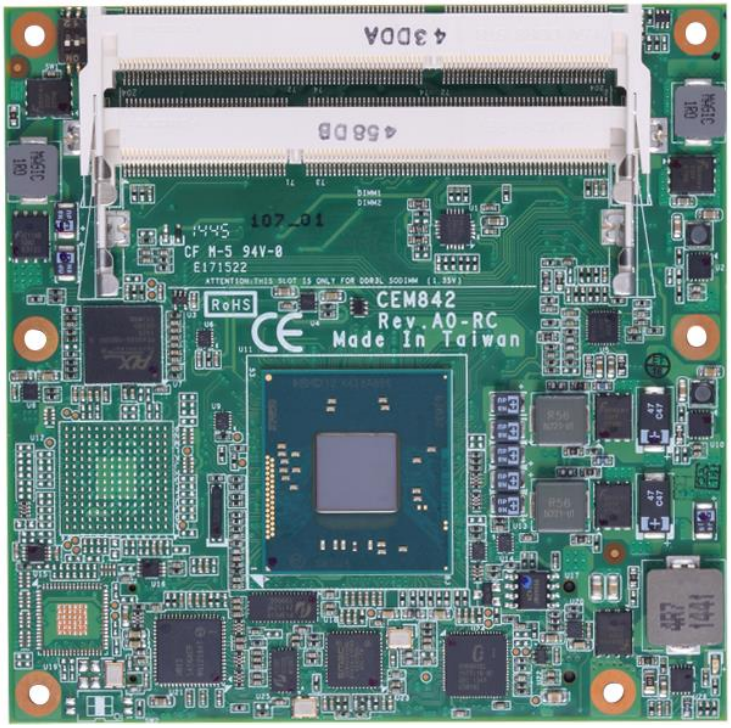
Chapter 1
Introduction



The CEM842 is a new COM Express™ Type 6 Compact Module supporting Intel® Celeron® quad/dual core J1900/N2807. Meanwhile, CEM843 is a new COM Express™ Type 6 Compact Module supporting Intel® Atom™ quad core E3845. Both of them deliver outstanding system performance and support excellent multiple I/Os like LVDS, one Gigabit Ethernet, HD Audio interface, two SATA-300, one USB 3.0 and eight USB 2.0 ports to make all in one single module as computing engine. For extension purpose, it provides maximum up to 6 lanes of PCI-Express Gen 2 at 5GT/s.

1.1 Features

- CEM842: Intel® Celeron® J1900/N2807 processors
- CEM843: Intel® Atom™ E3845 processor
- Two 204-pin SO-DIMMs supporting up to 8GB memory capacity
- Support max. up to 6 lanes of PCI-Express
- 2 SATA-300
- 1 USB 3.0 and 8 USB 2.0 ports

1.2 Specifications

- **CPU**
  - CEM842
    - Intel® Celeron® quad core J1900 2.0GHz
    - Intel® Celeron® dual core N2807 1.58GHz
  - CEM843
    - Intel® Atom™ quad core E3845 1.91GHz

- **BIOS**
  - American Megatrends Inc. BIOS.
  - 64Mbit SPI Flash, DMI, Plug and Play.
  - PXE Ethernet Boot ROM, customized default saving features, LPC-free supported, uses SPI type Flash memory.

- **System Memory**
  - Two 204-pin DDR3L 1333/1066MHz SO-DIMM sockets support maximum memory capacity up to 8GB.

Note

N2807 supports only one SO-DIMM socket (DIMM2).

- **Expansion Interface**
  - Six PCI-Express x1 or five PCI-Express x1 (while internal LAN is connected) routed through COM Express™ A_B connector.

- **USB Interface**
  - One USB port complies with USB Spec. Rev. 3.0.
  - Eight USB ports comply with USB Spec. Rev. 2.0.

Note

USB 2.0 port 4~7 do not support wake up function.

- **SATA Interface**
  - Two SATA 3Gb/s ports supported through COM Express™ connector.

- **Graphics**
  - Integrated in processor HD graphics Gen 7.
  - CRT interface supports up to 1920x1200.
  - 18/24-bit dual channel LVDS interface.
  - One DDI interface support DVI/HDMI/DisplayPort.

- **Ethernet**
  - CEM842 supports one 1000/100/10 Base-T provided by Intel® I210AT with integrated boot ROM.
  - CEM843 supports one 1000/100/10 Base-T provided by Intel® I210IT with integrated boot ROM.

- **Audio**
  - Intel® High Definition Audio interface.

- **Power Management**
  - ACPI (Advanced Configuration and Power Interface).

- **Form Factor**
  - Compact module 95mm x 95mm.

1.3 Utilities Supported

- Chipset driver
- Graphics driver
- Ethernet utility and driver
- Trusted execution engine
- Sideband fabric device
- USB 3.0 driver

Note

All specifications and images are subject to change without notice.

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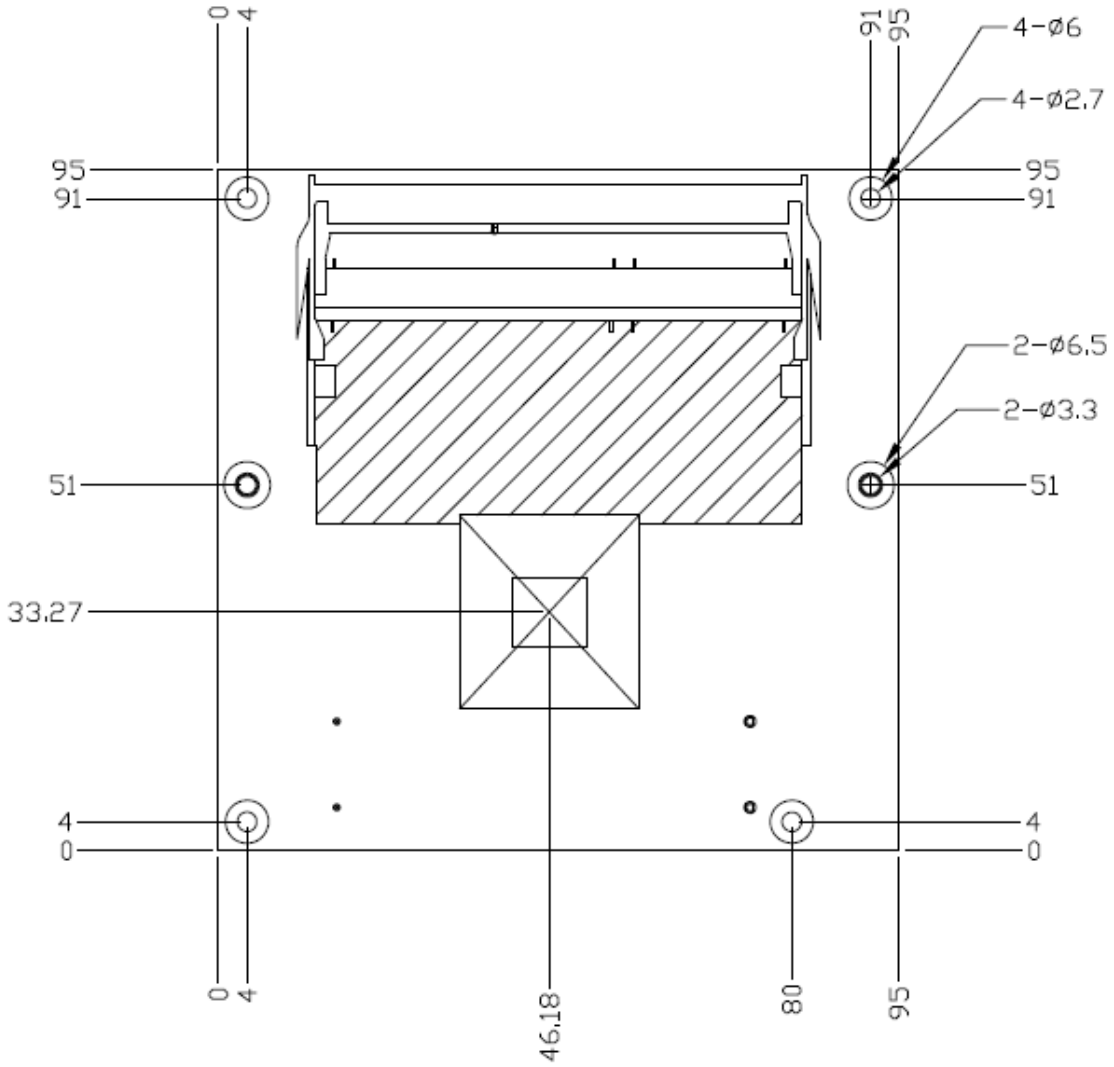
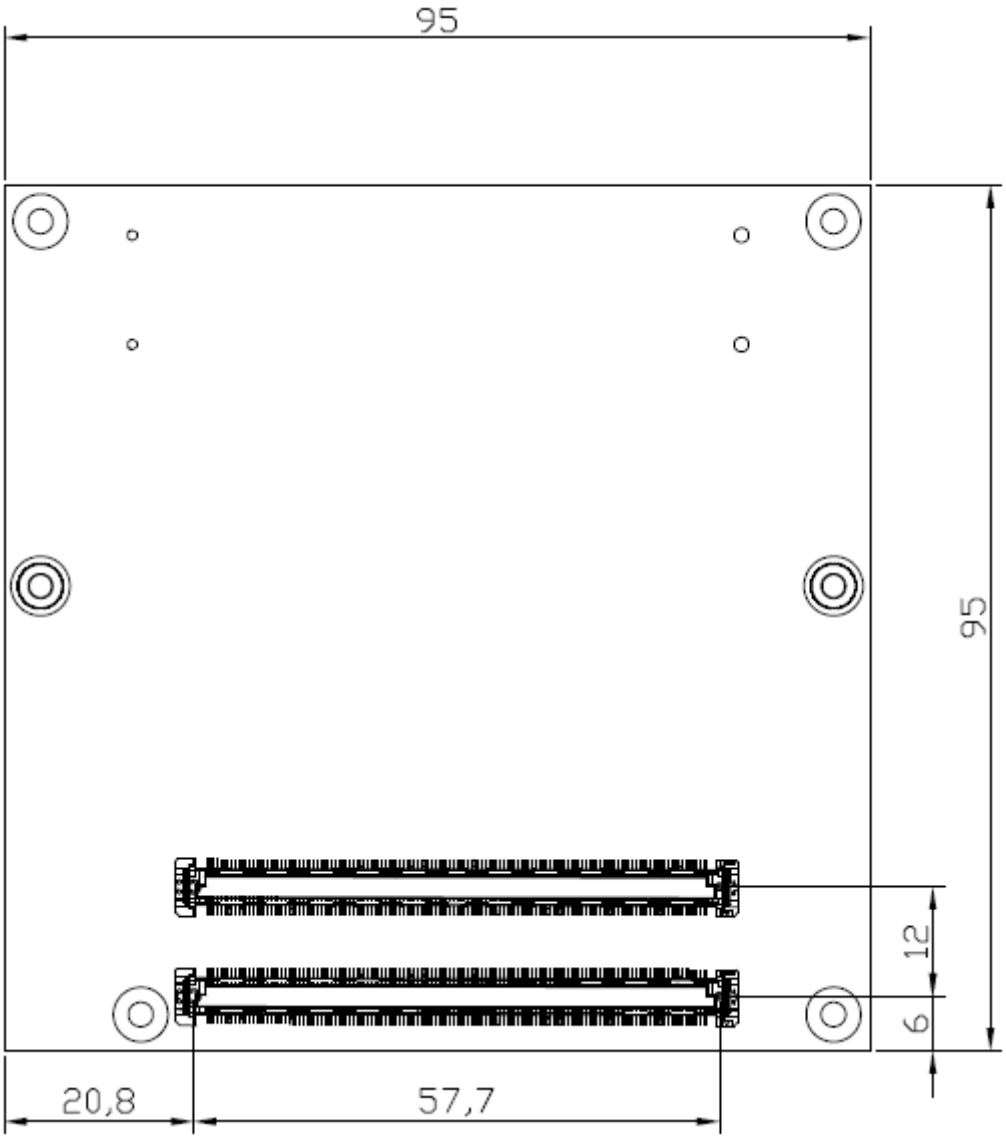
Chapter 2
Module and Pin Assignments

2.1 Module Dimensions and Fixing Holes

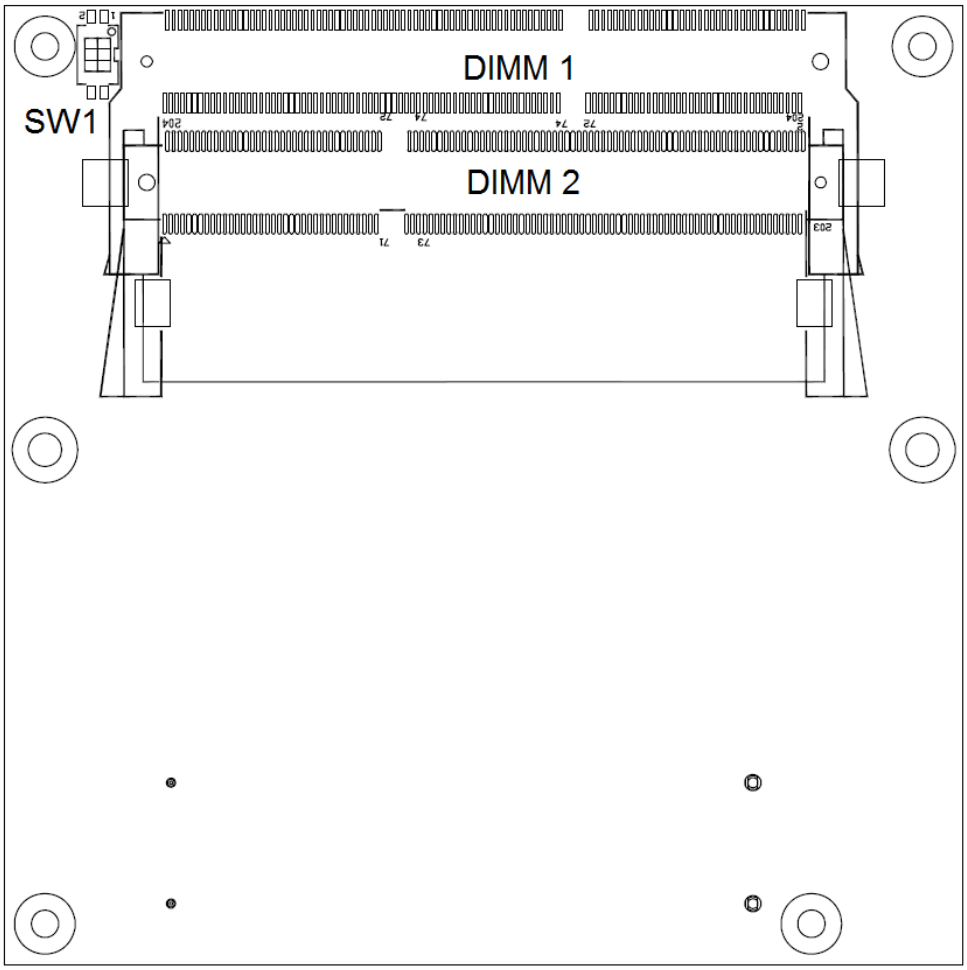


Top View

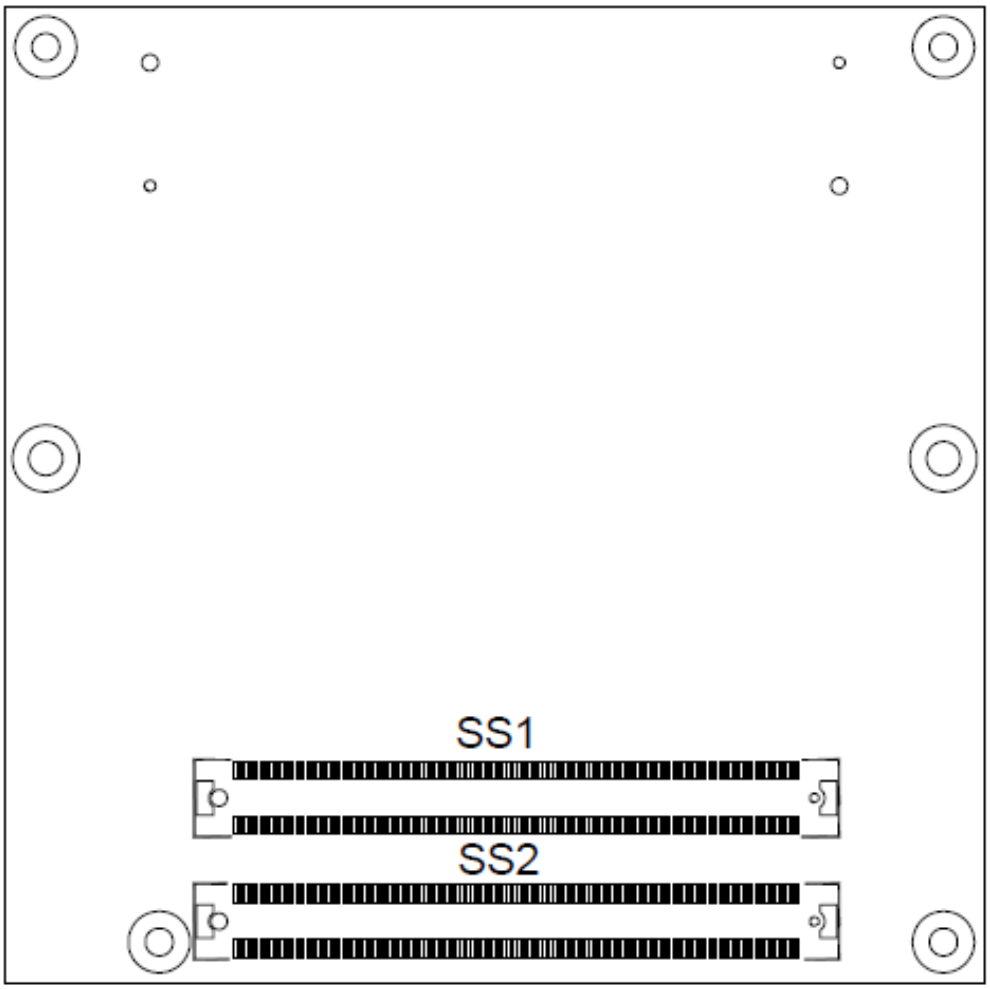


Bottom View

2.2 Module Layout



Top View



Bottom View

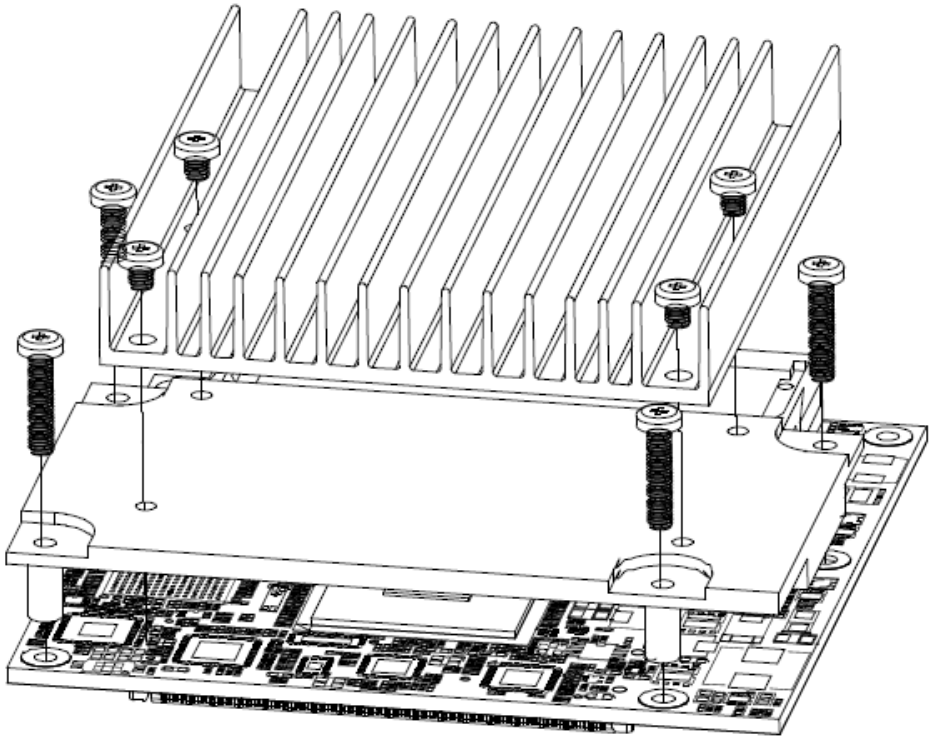
2.3 Installing Heatsink

For thermal dissipation, a thermal solution enables the CEM842/843's components to dissipate heat efficiently. All heat generating components are thermally conducted to the heatsink in order to avoid hot spots. Figure below illustrates how to install the thermal solution on CEM842/843.

1. There is a protective plastic covering on the thermal pads. This must be removed before the heatspreader can be mounted.

2. Each thermal solution is designed for a specific CEM module. The thermal pads on the heatspreader are designed to make contact with the necessary components on the CEM module. When mounting the heatspreader you must make sure that the thermal pads on the heatspreader make complete contact (no space between thermal pad and component) with the corresponding components on the CEM module. This is especially critical for CEM modules that have higher CPU speeds (for example 1.46GHz or more) to ensure that the heatspreader acts as a proper thermal interface for cooling solutions.

3. Before installing the heatspreader to the CPU module, please apply thermal grease on the CPU die. This CPU module has four assembly holes for installing heatspreader plate. Use the four screws to secure the heatspreader plate to the CEM842/843. Be careful not to over-tighten the screws. Then, apply thermal grease at the bottom of heatsink and secure the heatsink on the heatspreader by another four screws.



2.4 Switch Settings

Properly configure switch settings on the CEM842/843 to meet your application purpose. Below you can find a summary table of all switches and onboard default settings.

Note

Once the default switch setting needs to be changed, please do it under power-off condition.

Switch	Description	Setting
SW1	Auto Power On Default: Disable	SW1-1 OFF
	Restore BIOS Optimal Defaults Default: Normal Operation	SW1-2 OFF

2.4.1 Auto Power On and Restore BIOS Optimal Defaults (SW1)

If dip1 of SW1 (SW1-1) is set to ON position, the system will be automatically power on without pressing soft power button. If this jumper is set to OFF position, it is necessary to manually press soft power button to power on the system.

The dip2 of SW1 (SW1-2) is for restoring BIOS default status. Flip SW1-2 to ON position for a few seconds then flip it back to OFF position. Doing this procedure can restore BIOS optimal defaults.

Function	Setting
Disable auto power on (Default)	SW1-1 OFF
Enable auto power on	SW1-1 ON
Normal operation (Default)	SW1-2 OFF
Restore BIOS optimal defaults	SW1-2 ON

2.5 Connectors

Signals go to the other parts of the system through connectors. Loose or improper connection might cause problems, please make sure all connectors are properly and firmly connected. Here is a summary table which shows connectors on the hardware.

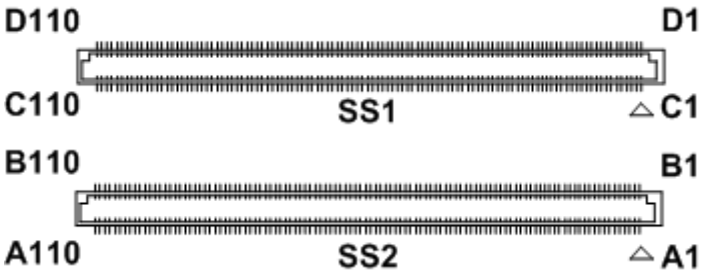
Connector	Description
DIMM1	Channel 1 DDR3L SO-DIMM Socket
DIMM2	Channel 0 DDR3L SO-DIMM Socket
SS1	COM Express™ Connector
SS2	COM Express™ Connector

Note

- ***For single memory channel configuration, install memory module in channel 0 DDR3L SO-DIMM socket (DIMM2).***
- ***For dual memory channel configuration, install memory modules of the same size, chip width, density and rank in channel 0 (DIMM2) and channel 1 (DIMM1) DDR3L SO-DIMM sockets.***

2.5.1 COM Express™ Connectors (SS1 and SS2)

The following table shows the pin assignments of the 220-pin COM Express™ connectors.



Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	GND	D2	GND
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	USB_SSRX0-	D3	USB_SSTX0-
A4	GBE0_LINK100#	B4	LPC_AD0	C4	USB_SSRX0+	D4	USB_SSTX0+
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	GND	D5	GND
A6	GBE0_MDI2-	B6	LPC_AD2	C6	N.C.	D6	N.C.
A7	GBE0_MDI2+	B7	LPC_AD3	C7	N.C.	D7	N.C.
A8	GBE0_LINK#	B8	N.C.	C8	GND	D8	GND
A9	GBE0_MDI1-	B9	N.C.	C9	N.C.	D9	N.C.
A10	GBE0_MDI1+	B10	LPC_CLK	C10	N.C.	D10	N.C.
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	N.C.	D12	N.C.
A13	GBE0_MDI0+	B13	SMB_CK	C13	N.C.	D13	N.C.
A14	GBE0_CTREF	B14	SMB_DAT	C14	GND	D14	GND
A15	SUS_S3#	B15	SMB_ALERT#	C15	N.C.	D15	DDI1_CTRLCLK_AUX+
A16	SATA0_TX+	B16	SATA1_TX+	C16	N.C.	D16	DDI1_CTRLDATA_AUX-
A17	SATA0_TX-	B17	SATA1_TX-	C17	N.C.	D17	N.C.
A18	SUS_S4#	B18	SUS_STAT#	C18	N.C.	D18	N.C.
A19	SATA0_RX+	B19	SATA1_RX+	C19	N.C.	D19	N.C.
A20	SATA0_RX-	B20	SATA1_RX-	C20	N.C.	D20	N.C.
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	N.C.	B22	N.C.	C22	N.C.	D22	N.C.
A23	N.C.	B23	N.C.	C23	N.C.	D23	N.C.
A24	SUS_S5#	B24	PWR_OK	C24	DDI1_HPD	D24	N.C.
A25	N.C.	B25	N.C.	C25	N.C.	D25	N.C.
A26	N.C.	B26	N.C.	C26	N.C.	D26	DDI1_PAIR0+
A27	BATLOW#	B27	WDT	C27	N.C.	D27	DDI1_PAIR0-
A28	(S)ATA_ACT#	B28	N.C.	C28	N.C.	D28	N.C.
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	C29	N.C.	D29	DDI1_PAIR1+
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	C30	N.C.	D30	DDI1_PAIR1-
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC/HDA_BITCLK	B32	SPKR	C32	N.C.	D32	DDI1_PAIR2+
A33	AC/HDA_SDOUT	B33	N.C.	C33	N.C.	D33	DDI1_PAIR2-
A34	BIOS_DISABLE#	B34	N.C.	C34	N.C.	D34	DDI1_DDC_AUX_SEL
A35	N.C.	B35	THRM#	C35	N.C.	D35	N.C.
A36	USB6-	B36	USB7-	C36	N.C.	D36	DDI1_PAIR3+
A37	USB6+	B37	USB7+	C37	N.C.	D37	DDI1_PAIR3-
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	N.C	D38	N.C.
A39	USB4-	B39	USB5-	C39	N.C	D39	N.C.
A40	USB4+	B40	USB5+	C40	N.C	D40	N.C.
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	N.C	D42	N.C
A43	USB2+	B43	USB3+	C43	N.C	D43	N.C
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	N.C	D44	N.C
A45	USB0-	B45	USB1-	C45	N.C.	D45	N.C.
A46	USB0+	B46	USB1+	C46	N.C	D46	N.C
A47	VCC_RTC	B47	EXCD1_PERST#	C47	N.C	D47	N.C
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	C48	N.C.	D48	N.C.
A49	EXCD0_CPPE#	B49	SYS_RESET#	C49	N.C.	D49	N.C.
A50	LPC_SERIRQ	B50	CB_RESET#	C50	N.C.	D50	N.C.
A51	GND (FIXED)	B51	GND (FIXED)	C51	GND (FIXED)	D51	GND (FIXED)
A52	PCIE_TX5+ (optional)	B52	PCIE_RX5+ (optional)	C52	N.C.	D52	N.C.
A53	PCIE_TX5- (optional)	B53	PCIE_RX5- (optional)	C53	N.C.	D53	N.C.
A54	GPI0	B54	GPO1	C54	N.C.	D54	N.C.
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	N.C.	D55	N.C.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A56	PCIE_TX4-	B56	PCIE_RX4-	C56	N.C.	D56	N.C.
A57	GND	B57	GPO2	C57	N.C.	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	N.C.	D58	N.C.
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	N.C.	D59	N.C.
A60	GND (FIXED)	B60	GND (FIXED)	C60	GND (FIXED)	D60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	N.C.	D61	N.C.
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	N.C.	D62	N.C.
A63	GPI1	B63	GPO3	C63	N.C.	D63	N.C.
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	N.C.	D64	N.C.
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	N.C.	D65	N.C.
A66	GND	B66	WAKE0#	C66	N.C.	D66	N.C.
A67	GPI2	B67	WAKE1#	C67	N.C.	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	N.C.	D68	N.C.
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	N.C.	D69	N.C.
A70	GND(FIXED)	B70	GND(FIXED)	C70	GND(FIXED)	D70	GND(FIXED)
A71	LVDS_A0+	B71	LVDS_B0+	C71	N.C.	D71	N.C.
A72	LVDS_A0-	B72	LVDS_B0-	C72	N.C.	D72	N.C.
A73	LVDS_A1+	B73	LVDS_B1+	C73	N.C.	D73	N.C.
A74	LVDS_A1-	B74	LVDS_B1-	C74	N.C.	D74	N.C.
A75	LVDS_A2+	B75	LVDS_B2+	C75	N.C.	D75	N.C.
A76	LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN	B77	LVDS_B3+	C77	N.C.	D77	N.C.
A78	LVDS_A3+	B78	LVDS_B3-	C78	N.C.	D78	N.C.
A79	LVDS_A3-	B79	LVDS_BKLT_EN	C79	N.C.	D79	N.C.
A80	GND(FIXED)	B80	GND(FIXED)	C80	GND(FIXED)	D80	GND(FIXED)
A81	LVDS_A_CK+	B81	LVDS_B_CK+	C81	N.C.	D81	N.C.
A82	LVDS_A_CK-	B82	LVDS_B_CK-	C82	N.C.	D82	N.C.
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL	C83	N.C.	D83	N.C.
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	N.C.	D85	N.C.
A86	N.C.	B86	VCC_5V_SBY	C86	N.C.	D86	N.C.
A87	N.C.	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE0_CK_REF+	B88	BIOS_DIS1	C88	N.C.	D88	N.C.
A89	PCIE0_CK_REF-	B89	VGA_RED	C89	N.C.	D89	N.C.
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	SPI_POWER	B91	VGA_GRN	C91	N.C.	D91	N.C.
A92	SPI_MISO	B92	VGA_BLU	C92	N.C.	D92	N.C.
A93	GPO0	B93	VGA_HSYNC	C93	GND	D93	GND
A94	SPI_CLK	B94	VGA_VSYNC	C94	N.C.	D94	N.C.
A95	SPI_MOSI	B95	VGA_I2C_CK	C95	N.C.	D95	N.C.
A96	TPM_PP	B96	VGA_I2C_DAT	C96	GND	D96	GND
A97	N.C.	B97	SPI_CS#	C97	N.C.	D97	N.C.
A98	N.C.	B98	N.C.	C98	N.C.	D98	N.C.
A99	N.C.	B99	N.C.	C99	N.C.	D99	N.C.
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	N.C.	B101	FAN_PWMOUT	C101	N.C.	D101	N.C.
A102	N.C.	B102	FAN_TACHIN	C102	N.C.	D102	N.C.
A103	LID#	B103	SLEEP#	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

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Chapter 3
Hardware Description

3.1 Microprocessor

The CEM842/843 supports Intel® Celeron® J1900/N2807 and Atom™ E3845 processors which enable your system to operate under Windows® 7, Windows® 8 and Linux environments. The system performance depends on the microprocessor. You must install the heatsink or cooler carefully and properly to prevent damage.

3.2 BIOS

The CEM842/843 uses AMI Plug and Play BIOS with a single 64Mbit SPI Flash.

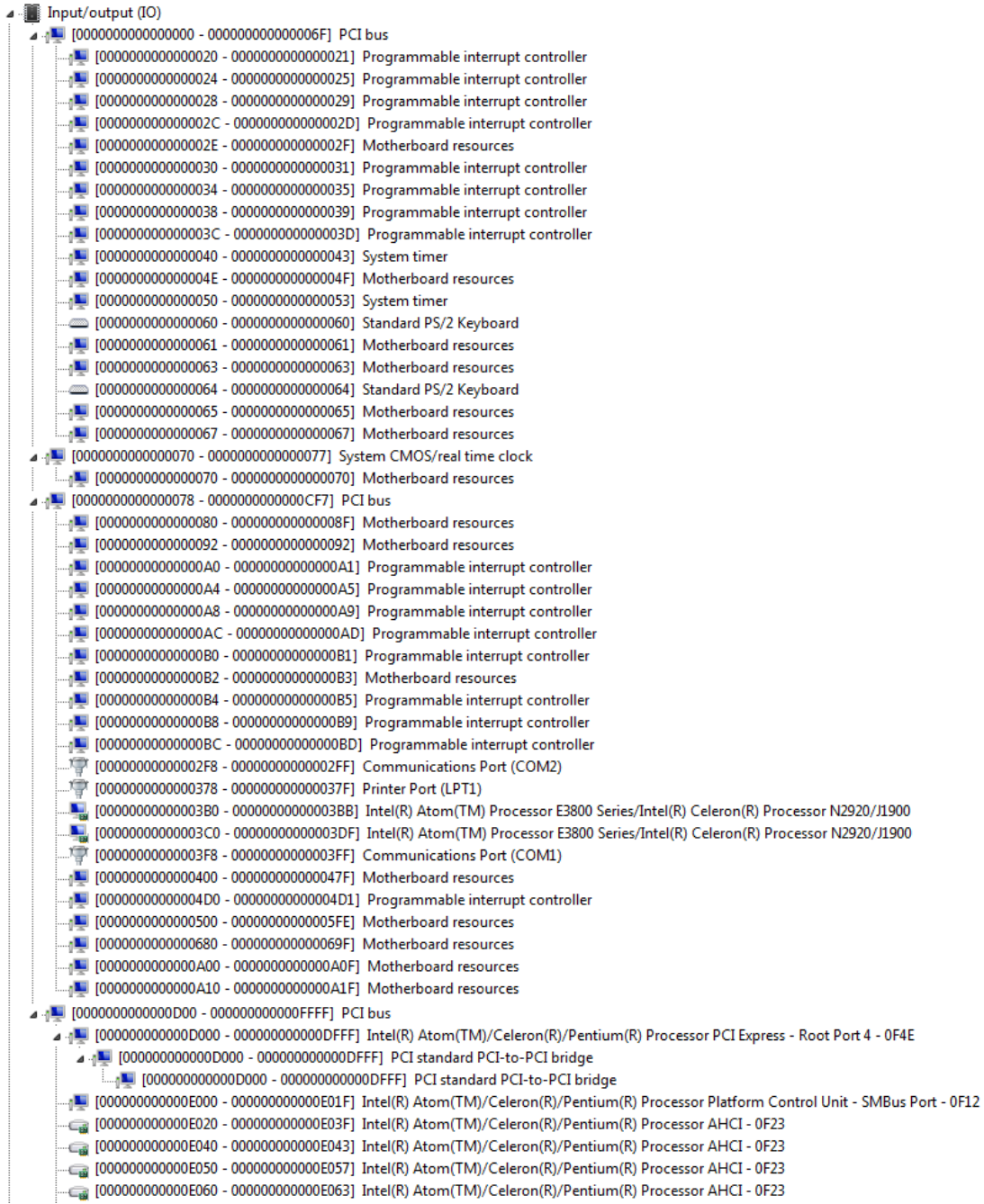
3.3 System Memory

The CEM842/843 supports two 204-pin DDR3L SO-DIMM sockets for maximum memory capacity up to 8GB DDR3L SDRAMs. The memory module comes in sizes of 1GB, 2GB, 4GB or 8GB.

3.4 I/O Port Address Map

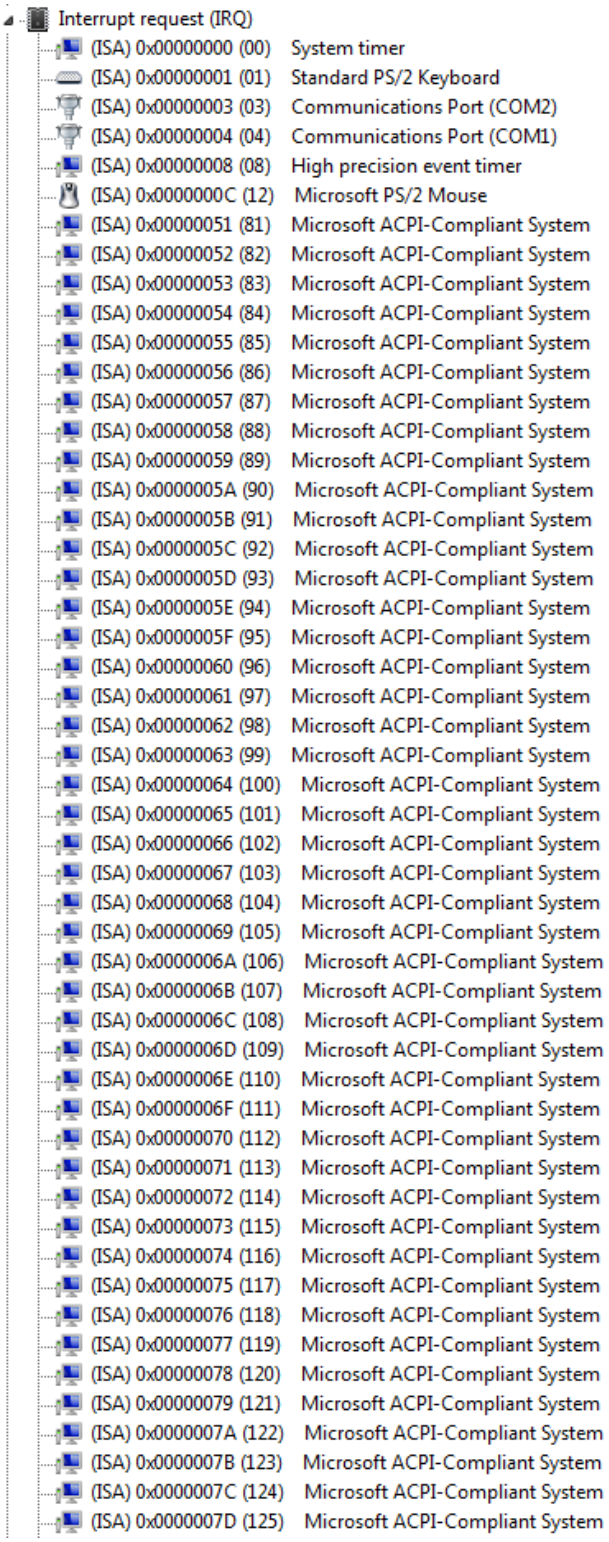
The Intel® Celeron® J1900/N2807 and Atom™ E3845 processors communicate via I/O ports. The I/O port addresses are available for assigning to other devices via I/O expansion cards.

The I/O port addresses (with CEB94006 baseboard under Windows® 7) are as follows:

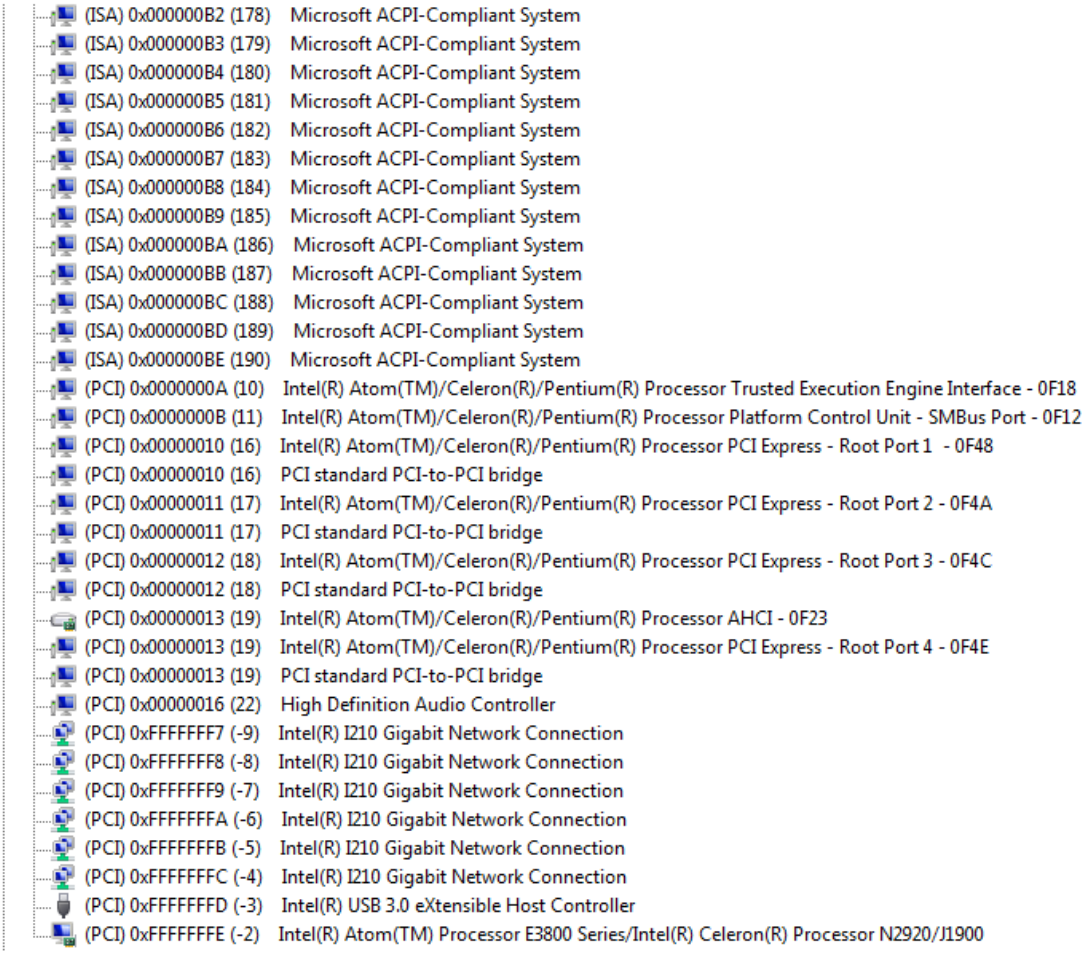


3.5 Interrupt Controller (IRQ) Map

The interrupt controller (IRQ) mapping list (with CEB94006 baseboard under Windows® 7) is shown as follows:

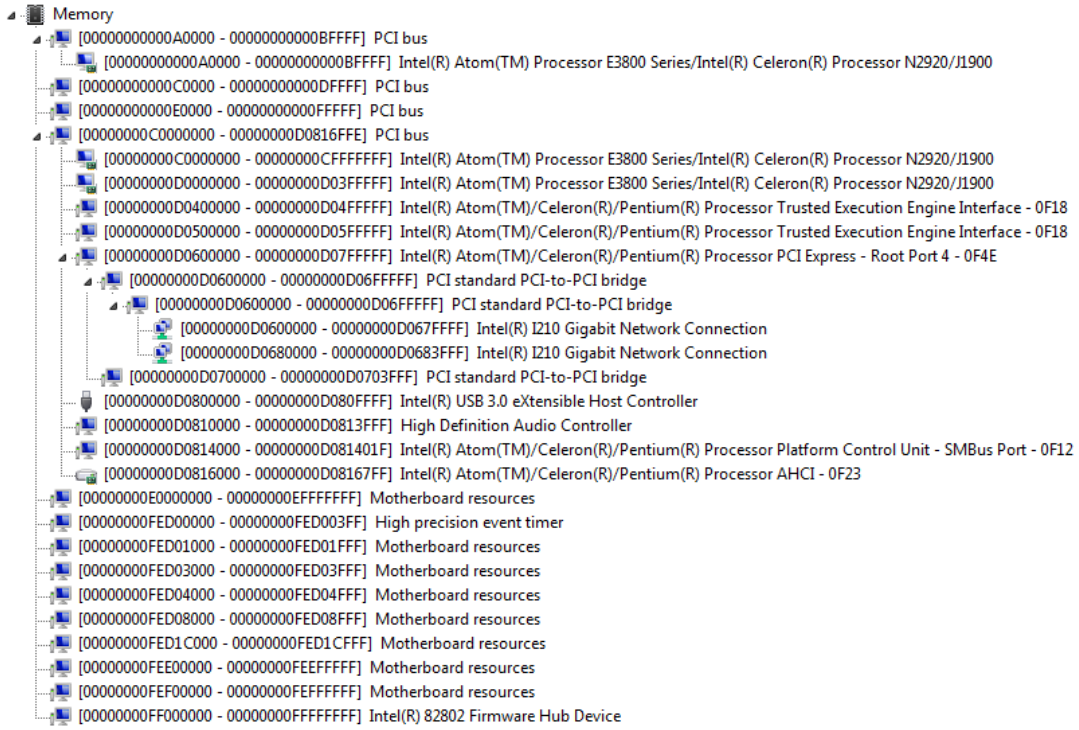


- (ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
- (ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
- (ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
- (ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
- (ISA) 0x00000082 (130) Microsoft ACPI-Compliant System
- (ISA) 0x00000083 (131) Microsoft ACPI-Compliant System
- (ISA) 0x00000084 (132) Microsoft ACPI-Compliant System
- (ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
- (ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
- (ISA) 0x00000087 (135) Microsoft ACPI-Compliant System
- (ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
- (ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
- (ISA) 0x0000008A (138) Microsoft ACPI-Compliant System
- (ISA) 0x0000008B (139) Microsoft ACPI-Compliant System
- (ISA) 0x0000008C (140) Microsoft ACPI-Compliant System
- (ISA) 0x0000008D (141) Microsoft ACPI-Compliant System
- (ISA) 0x0000008E (142) Microsoft ACPI-Compliant System
- (ISA) 0x0000008F (143) Microsoft ACPI-Compliant System
- (ISA) 0x00000090 (144) Microsoft ACPI-Compliant System
- (ISA) 0x00000091 (145) Microsoft ACPI-Compliant System
- (ISA) 0x00000092 (146) Microsoft ACPI-Compliant System
- (ISA) 0x00000093 (147) Microsoft ACPI-Compliant System
- (ISA) 0x00000094 (148) Microsoft ACPI-Compliant System
- (ISA) 0x00000095 (149) Microsoft ACPI-Compliant System
- (ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
- (ISA) 0x00000097 (151) Microsoft ACPI-Compliant System
- (ISA) 0x00000098 (152) Microsoft ACPI-Compliant System
- (ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
- (ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
- (ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
- (ISA) 0x0000009C (156) Microsoft ACPI-Compliant System
- (ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
- (ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
- (ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
- (ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System
- (ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
- (ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
- (ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System
- (ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
- (ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
- (ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System
- (ISA) 0x000000A7 (167) Microsoft ACPI-Compliant System
- (ISA) 0x000000A8 (168) Microsoft ACPI-Compliant System
- (ISA) 0x000000A9 (169) Microsoft ACPI-Compliant System
- (ISA) 0x000000AA (170) Microsoft ACPI-Compliant System
- (ISA) 0x000000AB (171) Microsoft ACPI-Compliant System
- (ISA) 0x000000AC (172) Microsoft ACPI-Compliant System
- (ISA) 0x000000AD (173) Microsoft ACPI-Compliant System
- (ISA) 0x000000AE (174) Microsoft ACPI-Compliant System
- (ISA) 0x000000AF (175) Microsoft ACPI-Compliant System
- (ISA) 0x000000B0 (176) Microsoft ACPI-Compliant System
- (ISA) 0x000000B1 (177) Microsoft ACPI-Compliant System


(ISA) 0x000000B2 (178) Microsoft ACPI-Compliant System
(ISA) 0x000000B3 (179) Microsoft ACPI-Compliant System
(ISA) 0x000000B4 (180) Microsoft ACPI-Compliant System
(ISA) 0x000000B5 (181) Microsoft ACPI-Compliant System
(ISA) 0x000000B6 (182) Microsoft ACPI-Compliant System
(ISA) 0x000000B7 (183) Microsoft ACPI-Compliant System
(ISA) 0x000000B8 (184) Microsoft ACPI-Compliant System
(ISA) 0x000000B9 (185) Microsoft ACPI-Compliant System
(ISA) 0x000000BA (186) Microsoft ACPI-Compliant System
(ISA) 0x000000BB (187) Microsoft ACPI-Compliant System
(ISA) 0x000000BC (188) Microsoft ACPI-Compliant System
(ISA) 0x000000BD (189) Microsoft ACPI-Compliant System
(ISA) 0x000000BE (190) Microsoft ACPI-Compliant System
(PCI) 0x0000000A (10) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor Trusted Execution Engine Interface - 0F18
(PCI) 0x0000000B (11) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor Platform Control Unit - SMBus Port - 0F12
(PCI) 0x00000010 (16) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 1 - 0F48
(PCI) 0x00000010 (16) PCI standard PCI-to-PCI bridge
(PCI) 0x00000011 (17) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 2 - 0F4A
(PCI) 0x00000011 (17) PCI standard PCI-to-PCI bridge
(PCI) 0x00000012 (18) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 3 - 0F4C
(PCI) 0x00000012 (18) PCI standard PCI-to-PCI bridge
(PCI) 0x00000013 (19) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor AHCI - 0F23
(PCI) 0x00000013 (19) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 4 - 0F4E
(PCI) 0x00000013 (19) PCI standard PCI-to-PCI bridge
(PCI) 0x00000016 (22) High Definition Audio Controller
(PCI) 0xFFFFFFF7 (-9) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFF8 (-8) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFF9 (-7) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFFA (-6) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFFB (-5) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFFC (-4) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFFD (-3) Intel(R) USB 3.0 eXtensible Host Controller
(PCI) 0xFFFFFFFE (-2) Intel(R) Atom(TM) Processor E3800 Series/Intel(R) Celeron(R) Processor N2920/J1900

3.6 Memory Map

The memory (with CEB94006 baseboard under Windows® 7) mapping list is shown as follows:



Chapter 4
AMI BIOS Setup Utility

The AMI UEFI BIOS provides users with a built-in setup program to modify basic system configuration. All configured parameters are stored in a flash chip to save the setup information whenever the power is turned off. This chapter provides users with detailed description about how to set up basic system configuration through the AMI BIOS setup utility.

4.1 Starting

To enter the setup screens, follow the steps below:

1. Turn on the computer and press the <Del> key immediately.
2. After you press the <Del> key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Advanced and Chipset menus.

Note

If your computer cannot boot after making and saving system changes with BIOS setup, you can restore BIOS optimal defaults by setting SW1-2 (see section 2.4.1).

It is strongly recommended that you should avoid changing the chipset's defaults. Both AMI and your system manufacturer have carefully set up these defaults that provide the best performance and reliability.

4.2 Navigation Keys

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F2>, <Enter>, <ESC>, <Arrow> keys, and so on.

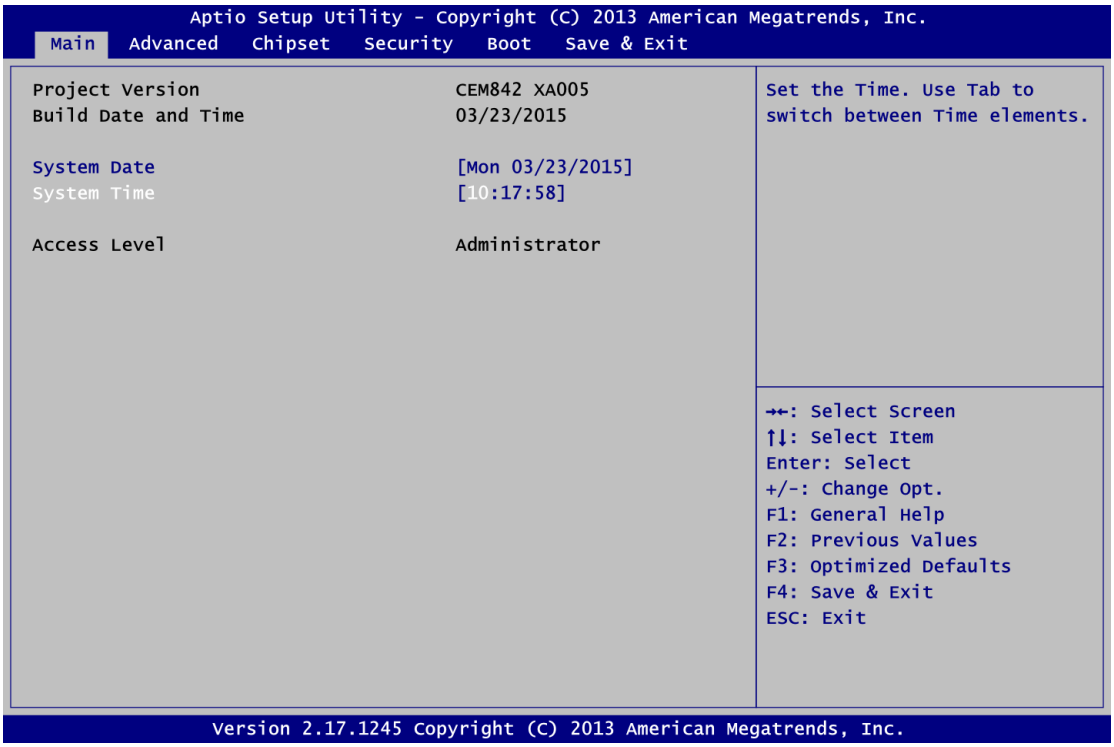
Note

Some of the navigation keys differ from one screen to another.

Hot Keys	Description
→← Left/Right	The Left and Right <Arrow> keys allow you to select a setup screen.
↑↓ Up/Down	The Up and Down <Arrow> keys allow you to select a setup screen or sub-screen.
+– Plus/Minus	The Plus and Minus <Arrow> keys allow you to change the field value of a particular setup item.
Tab	The <Tab> key allows you to select setup fields.
F1	The <F1> key allows you to display the General Help screen.
F2	The <F2> key allows you to Load Previous Values.
F3	The <F3> key allows you to Load Optimized Defaults.
F4	The <F4> key allows you to save any changes you have made and exit Setup. Press the <F4> key to save your changes.
Esc	The <Esc> key allows you to discard any changes you have made and exit the Setup. Press the <Esc> key to exit the setup without saving your changes.
Enter	The <Enter> key allows you to display or change the setup option listed for a particular setup item. The <Enter> key can also allow you to display the setup sub- screens.

4.3 Main Menu

When you first enter the setup utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. System Time/Date can be set up as described below. The Main BIOS setup screen is shown below.



BIOS Information
Display BIOS information.

System Date/Time
Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

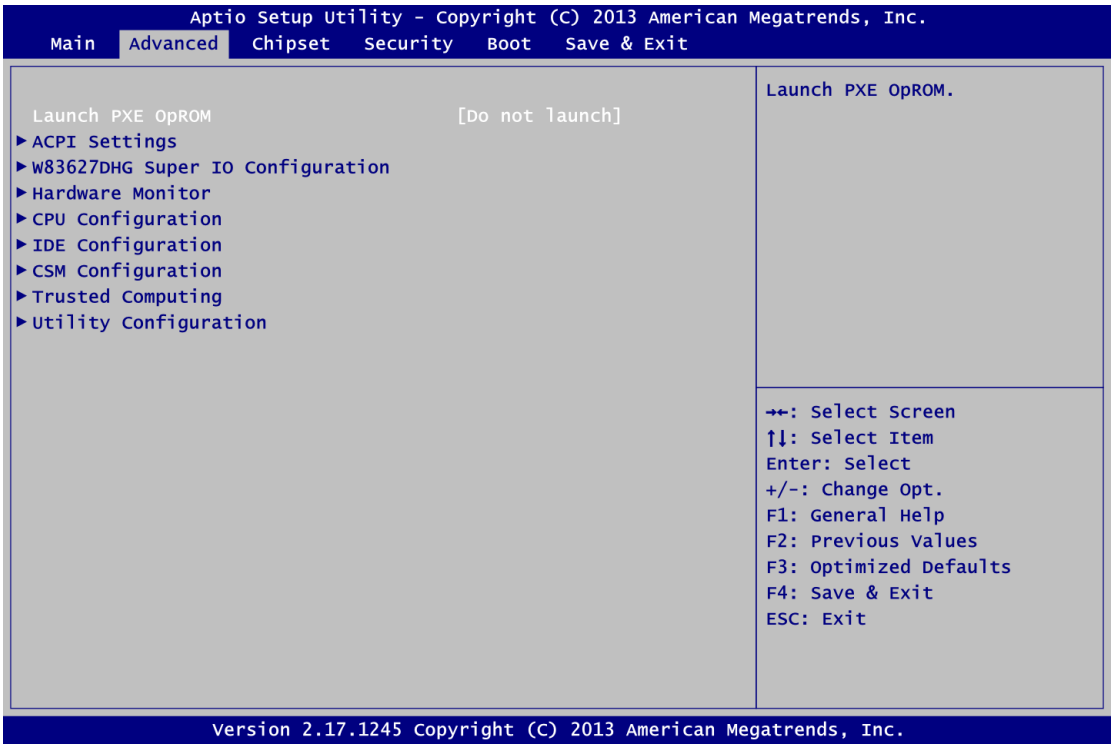
Access Level
Display the access level of current user.

4.4 Advanced Menu

The Advanced menu also allows users to set configuration of the CPU and other system devices. You can select any of the items in the left frame of the screen to go to the sub menus:

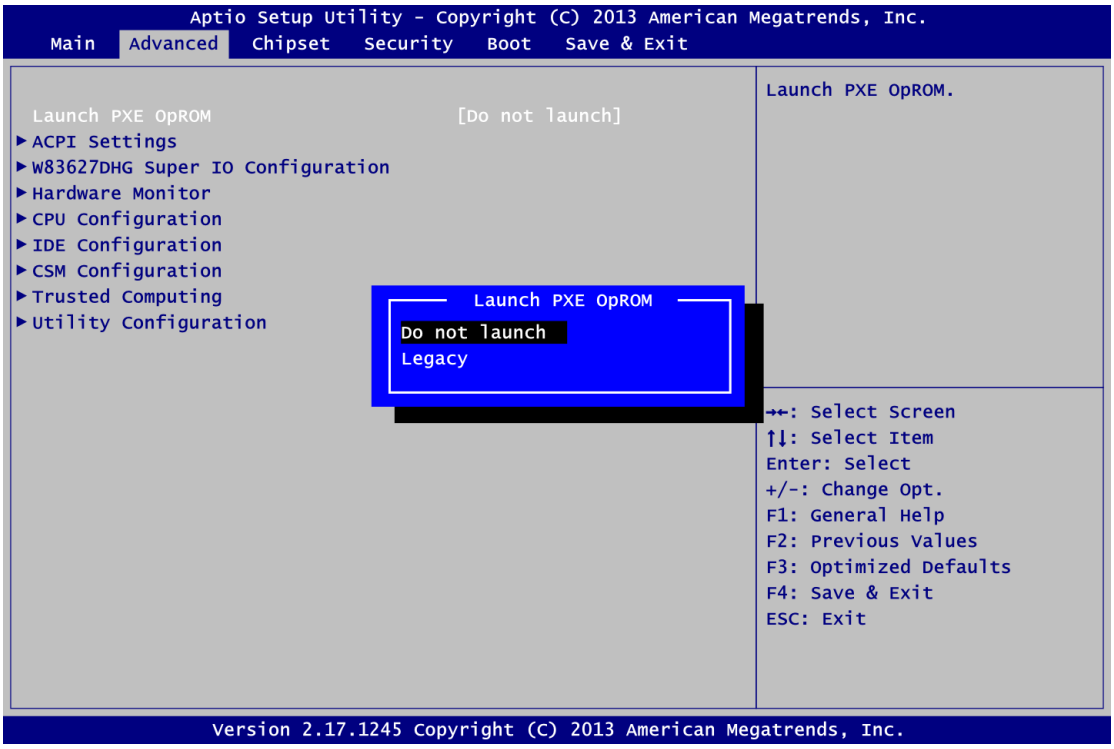
- ACPI Settings
- W83627DHG Super IO Configuration
- Hardware Monitor
- CPU Configuration
- IDE Configuration
- CSM Configuration
- Trusted Configuration
- Utility Configuration

For items marked with "►", please press <Enter> for more options.



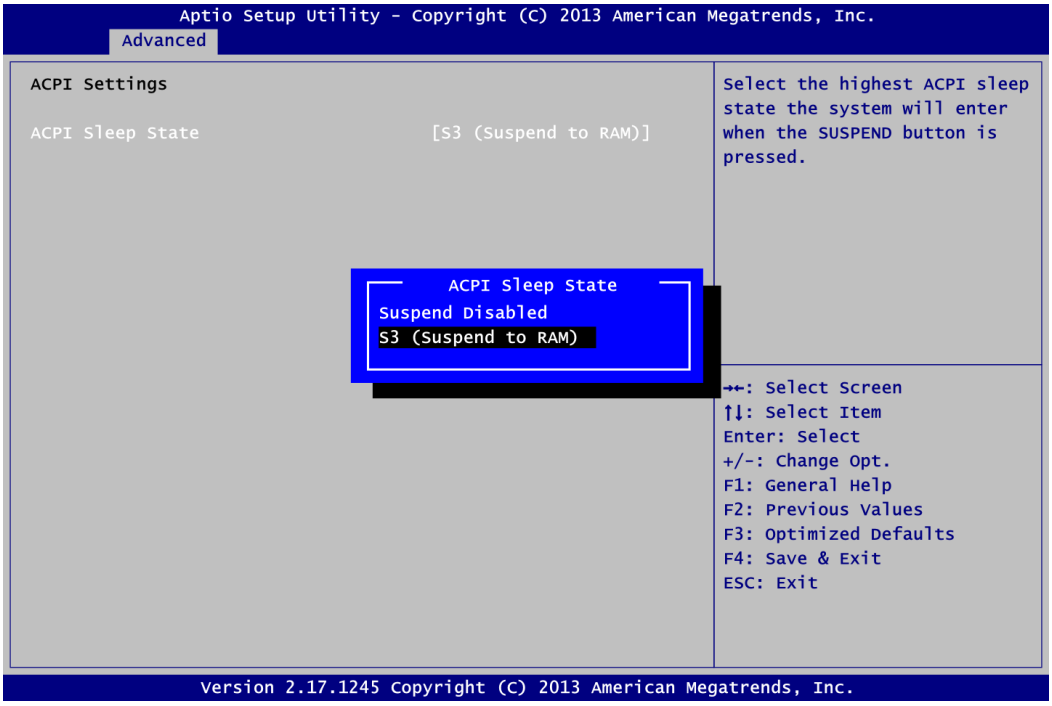
Note

W83627DHG Super IO configuration is applied on CEB94006.



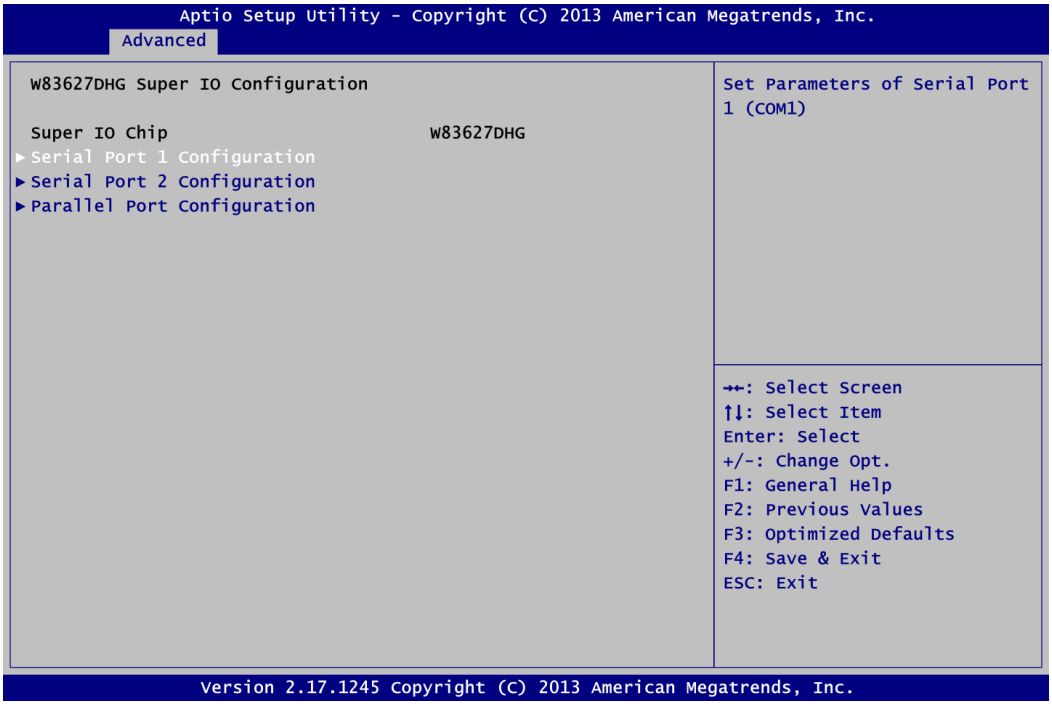
Launch PXE OpROM
Control the execution of legacy Preboot eXecution Environment (PXE) boot ROM function of the onboard LAN chip during system boots up.

- **ACPI Settings**
  You can use this screen to select options for the ACPI configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen.



ACPI Sleep State
Select the ACPI (Advanced Configuration and Power Interface) sleep state. Configuration options are Suspend Disabled and S3 (Suspend to RAM). The S3 (Suspend to RAM) option selects ACPI sleep state the system will enter when suspend button is pressed.

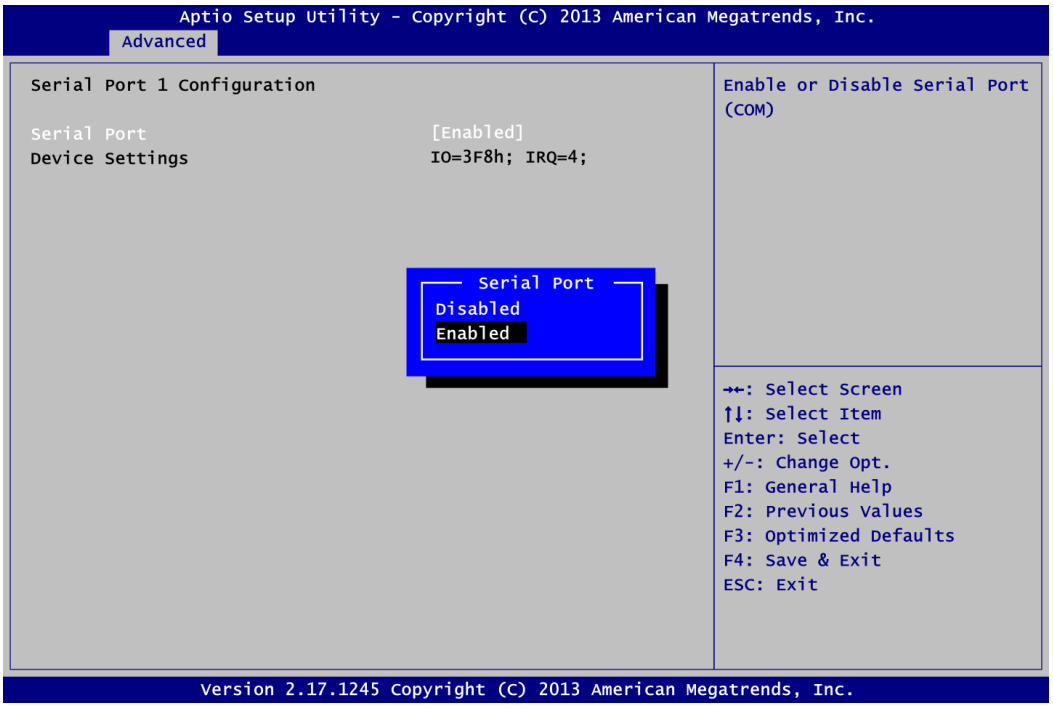
- **W83627DHG Super IO Configuration**
  You can use this screen to select options for the Super IO Configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen. For items marked with "►", please press <Enter> for more options.



Serial Port 1~2 Configuration
Set parameters of serial port 1~2 .

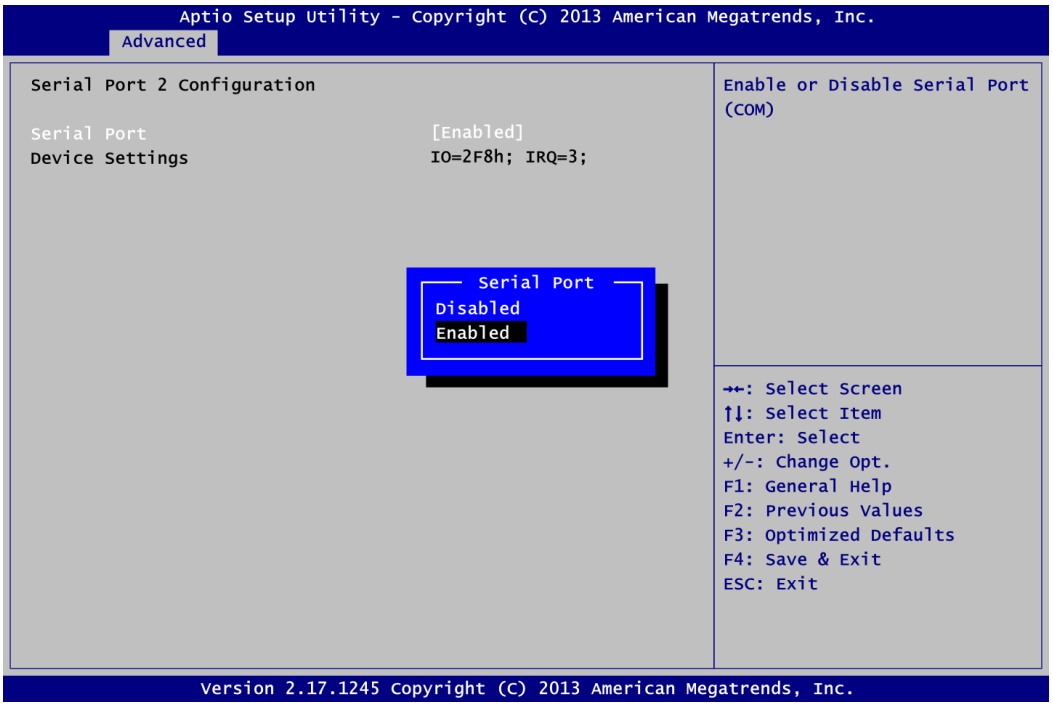
Parallel Port Configuration
Set parameters of parallel port.

- **Serial Port 1 Configuration**



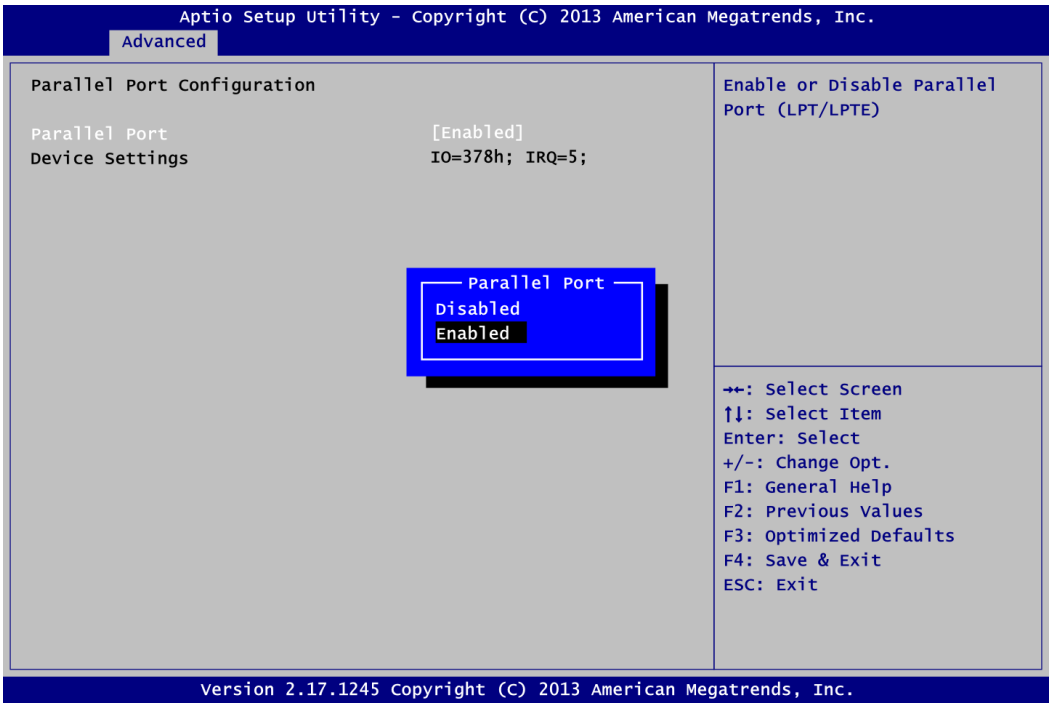
Serial Port
Enable or disable serial port 1. The optimal setting for base I/O address is 3F8h and for interrupt request line is IRQ4.

- **Serial Port 2 Configuration**



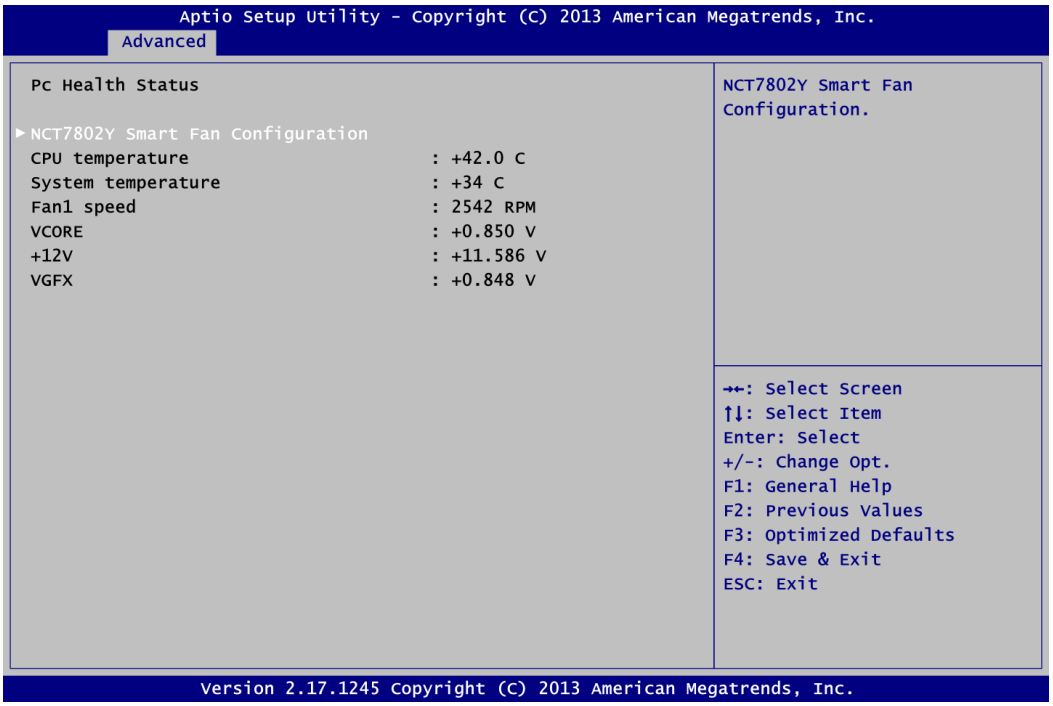
Serial Port
Enable or disable serial port 2. The optimal setting for base I/O address is 2F8h and for interrupt request line is IRQ3.

- **Parallel Port Configuration**

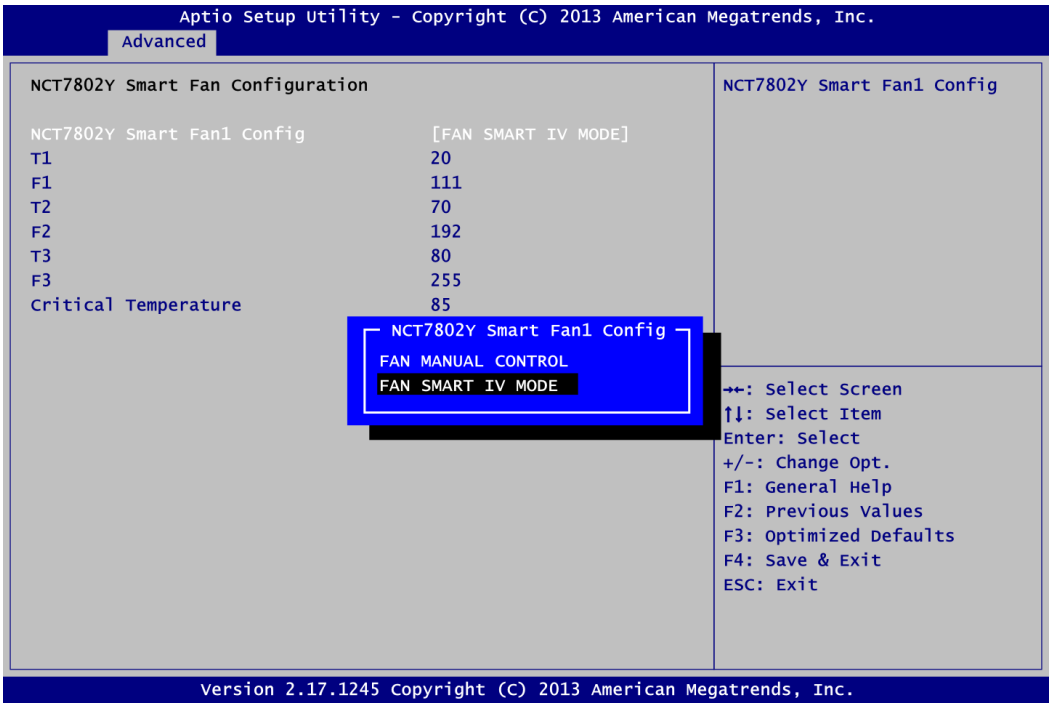


Parallel Port
Enable or disable parallel port (LPT). The optimal setting for base I/O address is 378h and for interrupt request line is IRQ5.

- **Hardware Monitor**
This screen is for hardware health status monitoring.

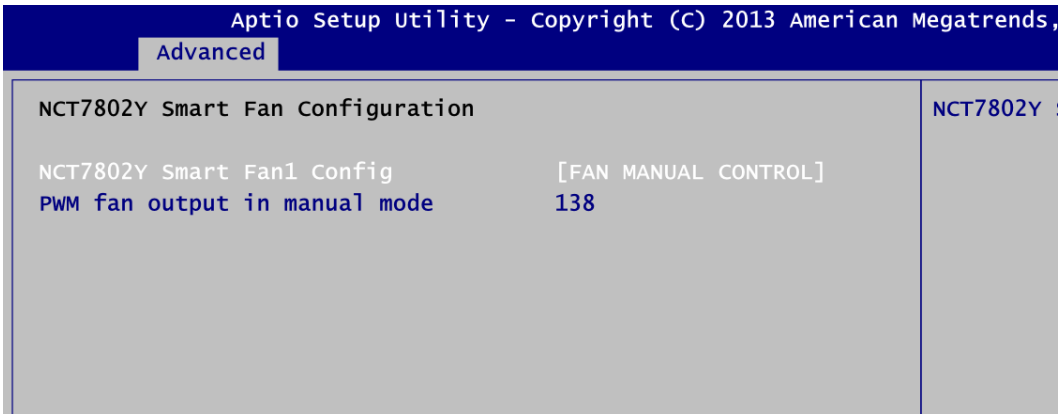


This screen displays the temperature of system and CPU, fan speed in RPM and system voltages (VCORE, +12V and VGFX).



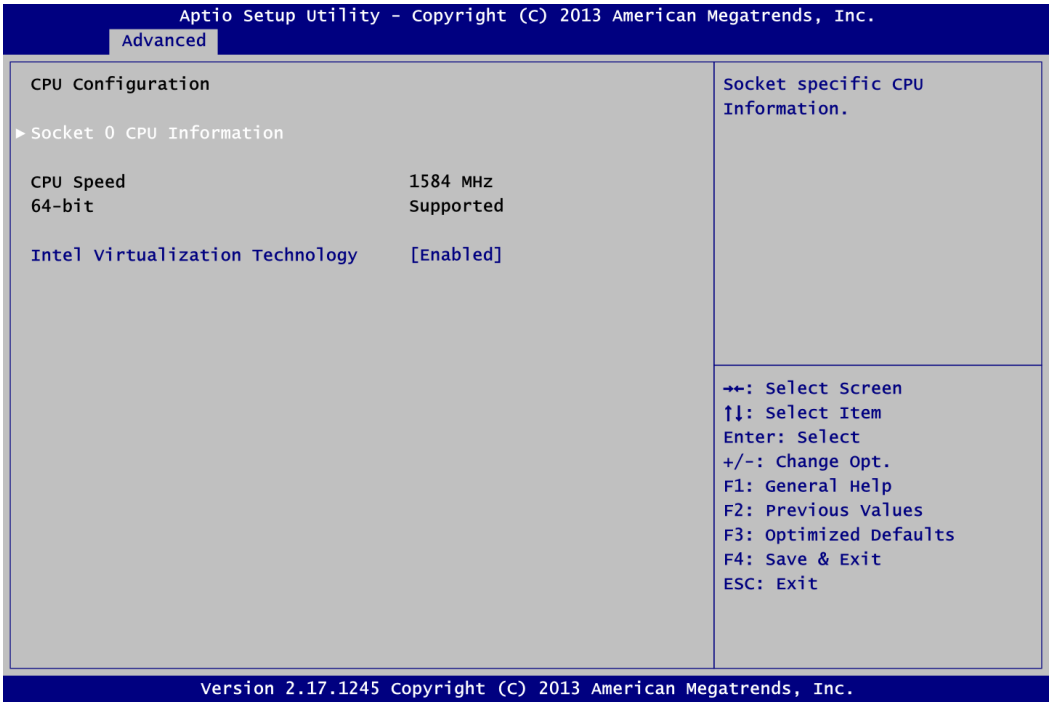
NCT7802Y Smart Fan1 Config

Smart Fan configuration provides two modes: FAN SMART IV MODE and FAN MANUAL CONTROL to control fan speed. In FAN SMART IV MODE, the fan speed is controlled by T1(temperature level1)/F1(fan duty 1), T2(temperature level2)/F2(fan duty 2) and T3(temperature level3)/F3(fan duty 3). Please base on the specification of the fan to set these parameters. We suggest that the range of fan duty is from 111 to 255. Setting the value of these parameters must follow T3>T2>T1 and F3>F2>F1. The default is FAN SMART IV MODE, and each default setting of temperature/fan duty is T1:20 F1:111, T2:70 F2:192, T3:80 F3:255.



In FAN MANUAL CONTROL mode, the fan speed is controlled by fan PWM duty and the range is from 111 to 255.

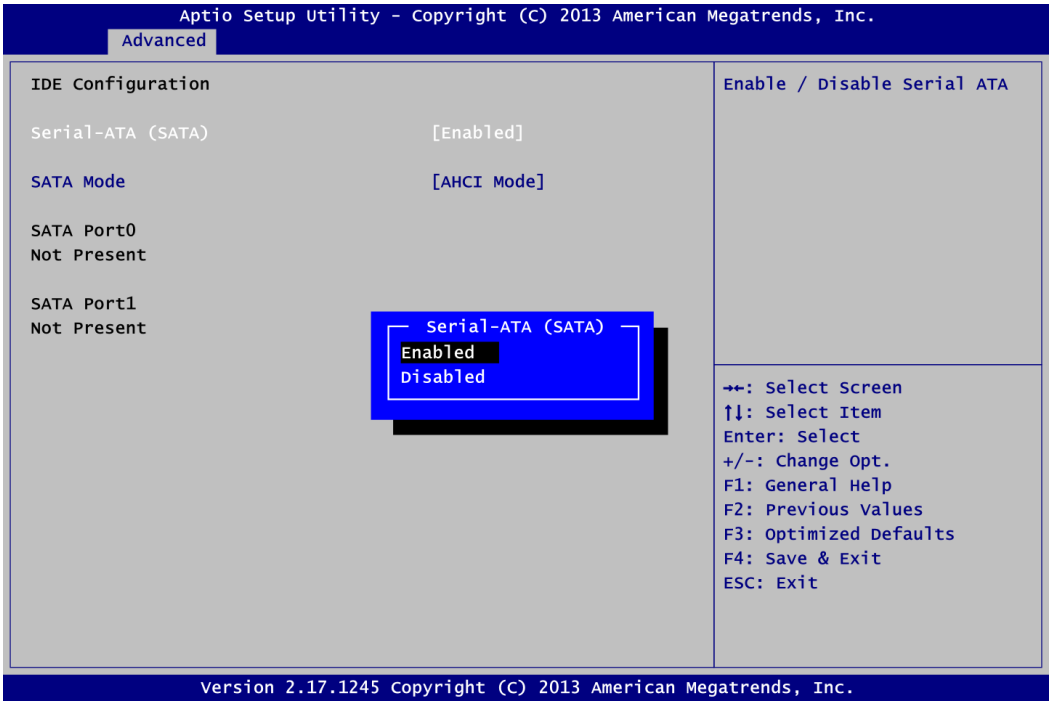
- **CPU Configuration**
  This screen shows the CPU Configuration, and you can change the value of the selected option.



Socket 0 CPU Information
Show CPU information.

Intel Virtualization Technology
Enable or disable Intel Virtualization Technology. When enabled, a VMM can utilize the additional hardware capabilities. It allows a platform to run multiple operating systems and applications independently, hence enabling a computer system to work as several virtual systems.

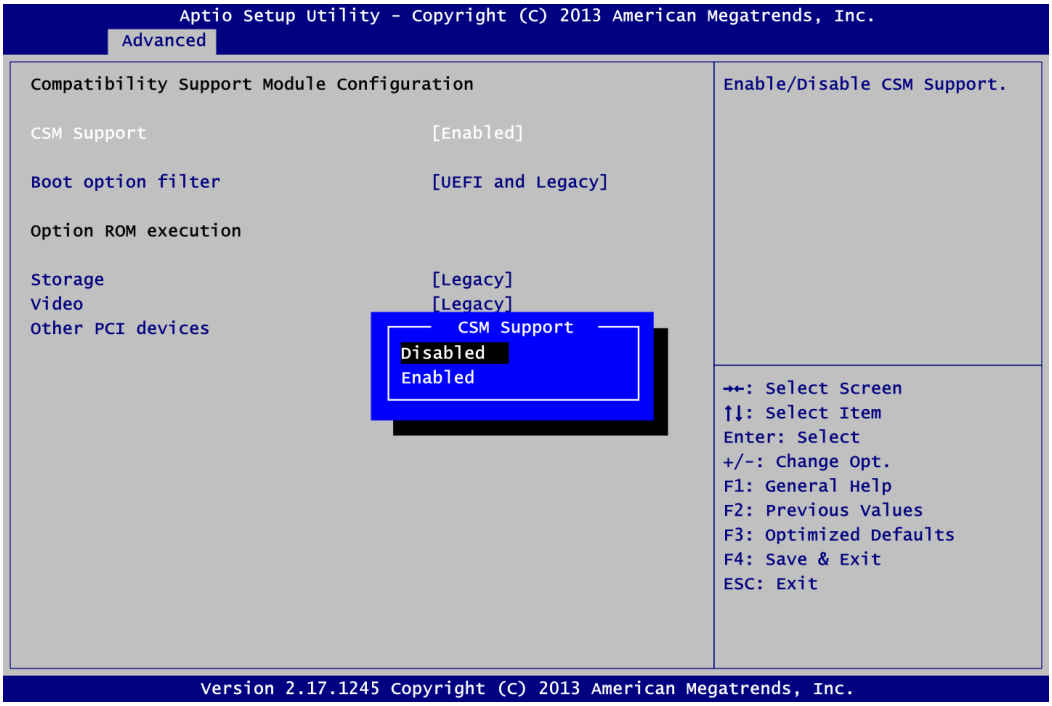
- **IDE Configuration**
  In the IDE Configuration menu, you can see the currently installed hardware in the SATA ports. During system boot up, the BIOS automatically detects the presence of SATA devices.



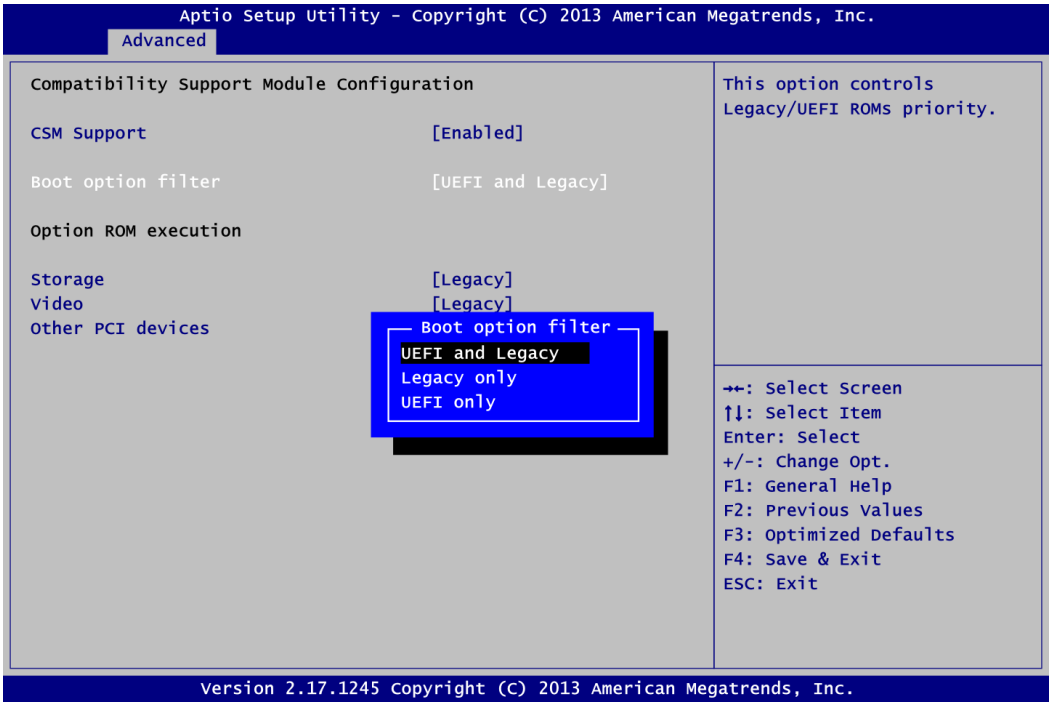
Serial-ATA (SATA)
Enable or disable SATA controller.

SATA Mode
Select what mode is operated on SATA controller. Operation modes are IDE Mode and AHCI Mode. Default is AHCI Mode.

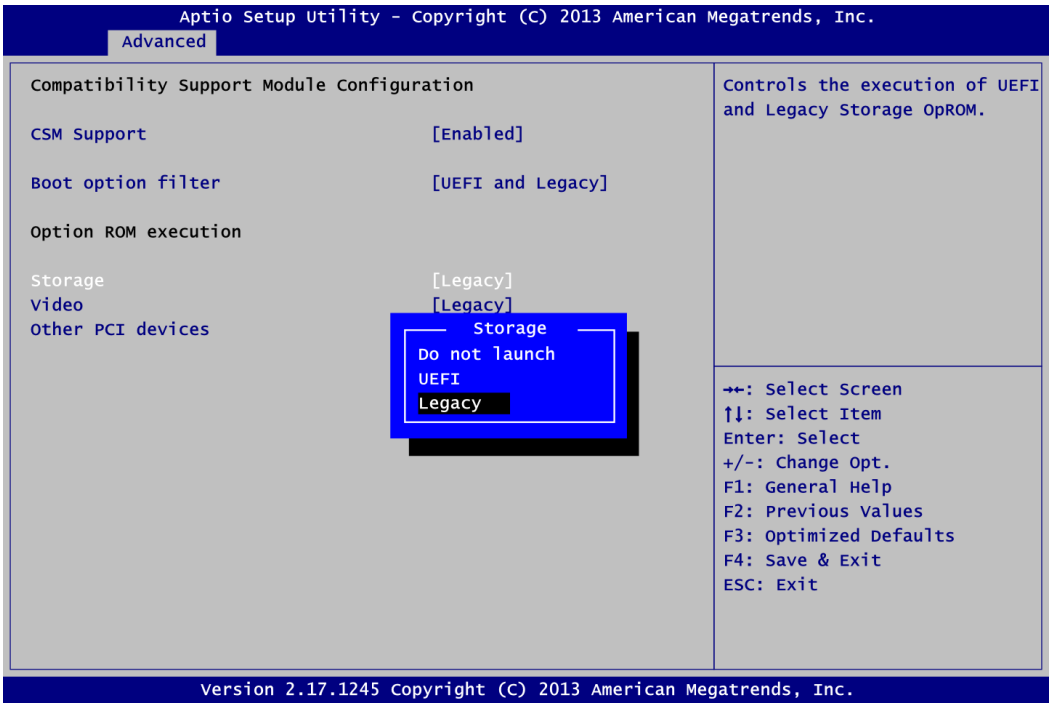
- **CSM Configuration**
  In the CSM (Compatibility Support Module) Configuration menu, you can enable or disable option ROM execution settings.



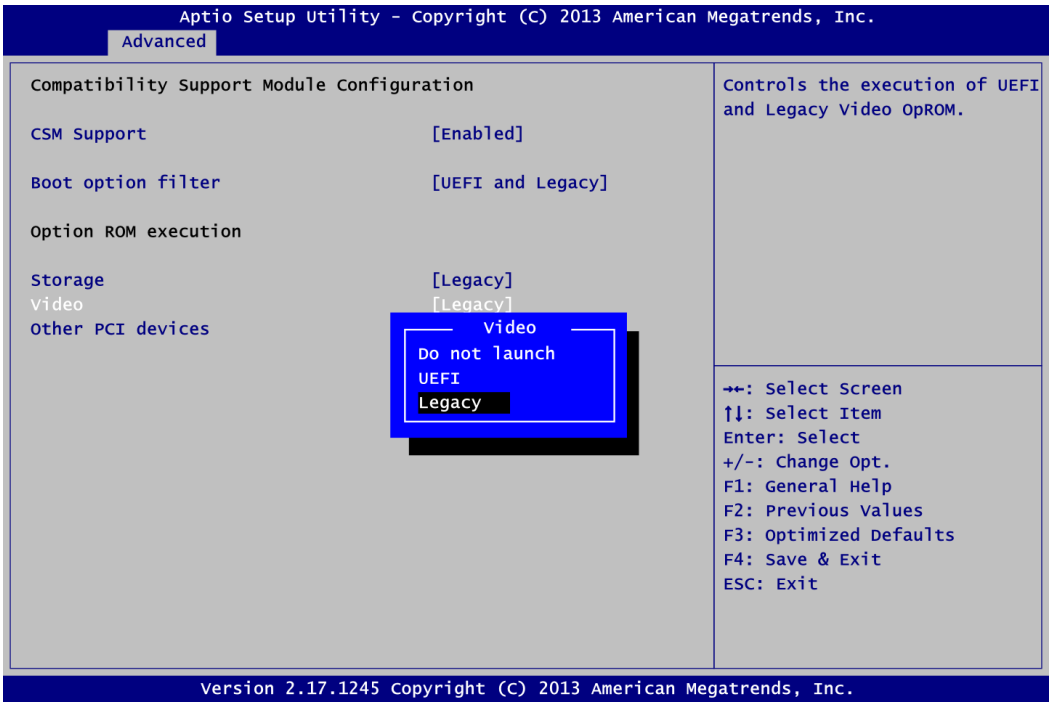
CSM support
Enable or disable CSM support.



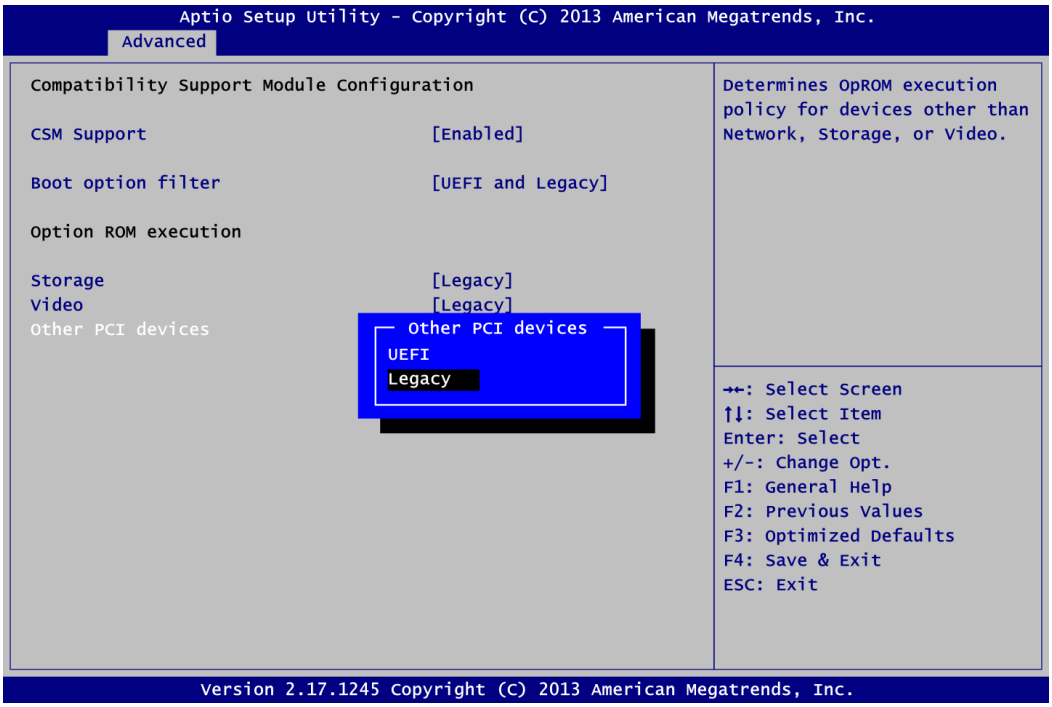
Boot option filter
Select UEFI or Legacy ROM priority. Default is UEFI and Legacy mode.



Storage
Select the execution of UEFI or Legacy storage option ROM. Default is Legacy mode.

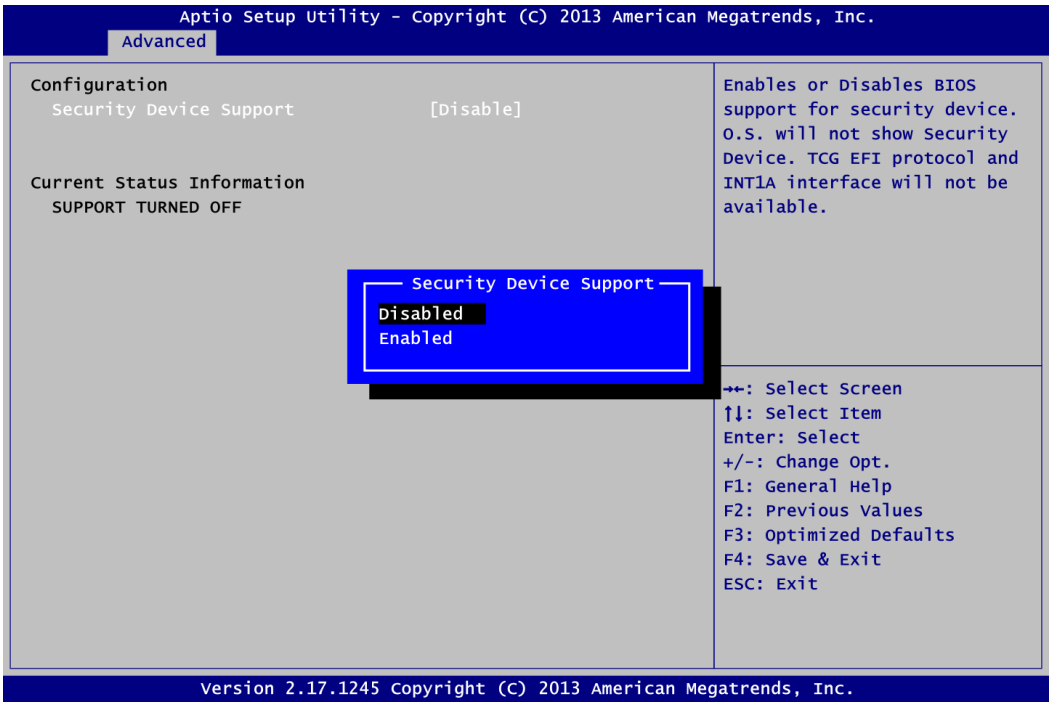


Video
Select the execution of UEFI or Legacy video option ROM. Default is Legacy mode.



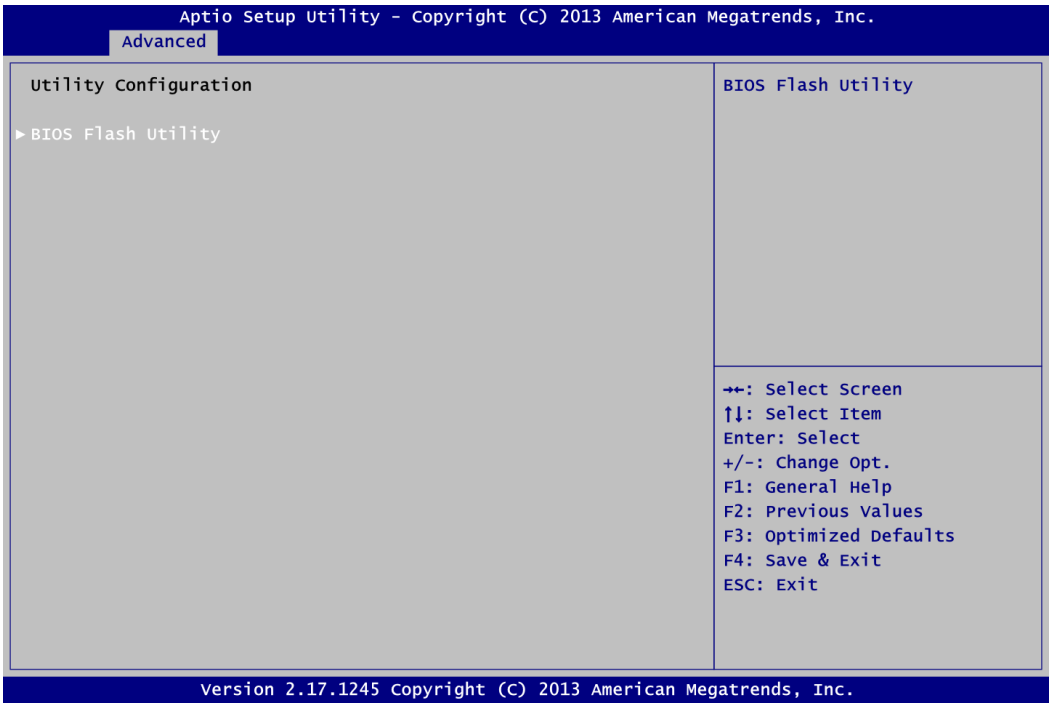
Other PCI devices
Select the execution of UEFI or Legacy option ROM of other PCIe network, storage or video devices. Default is Legacy mode.

- **Trusted Computing**
  You can use this screen for TPM (Trusted Platform Module) configuration. It also shows current TPM status information.



Security Device Support
Enable or disable BIOS support for security device. The default is Disabled.

- **Utility Configuration**



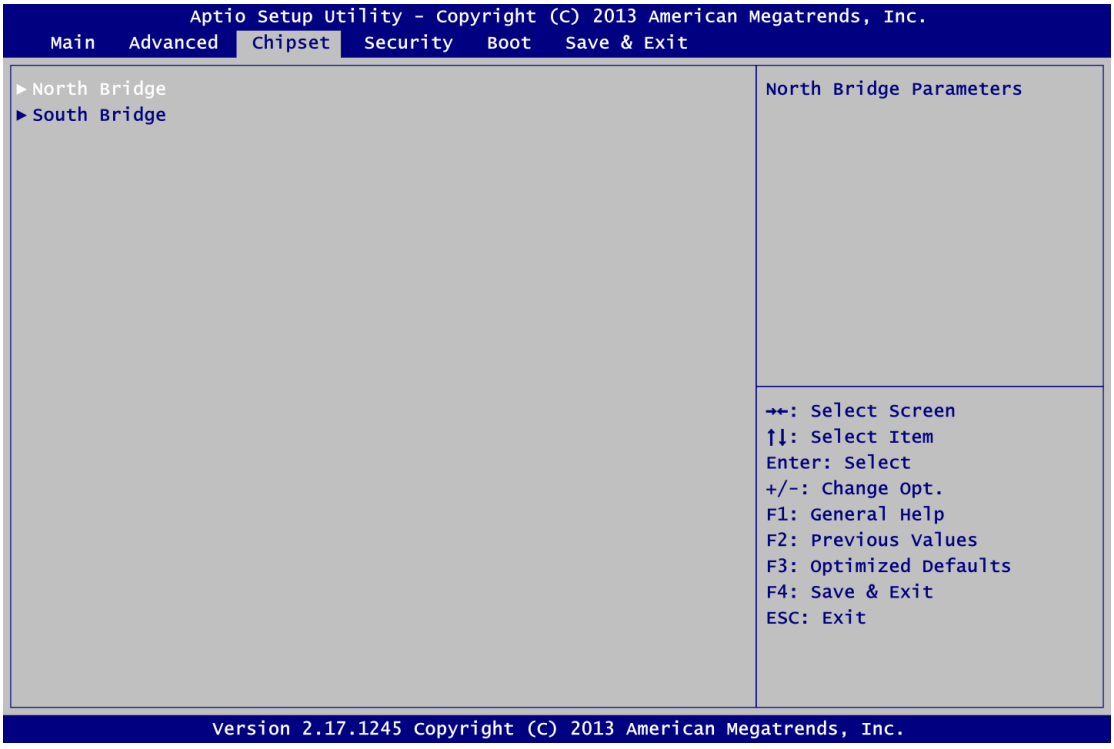
BIOS Flash Utility
BIOS flash utility configuration. For more detailed information, please refer to Appendix A.

4.5 Chipset Menu

The Chipset menu allows users to change the advanced chipset settings. You can select any of the items in the left frame of the screen to go to the sub menus:

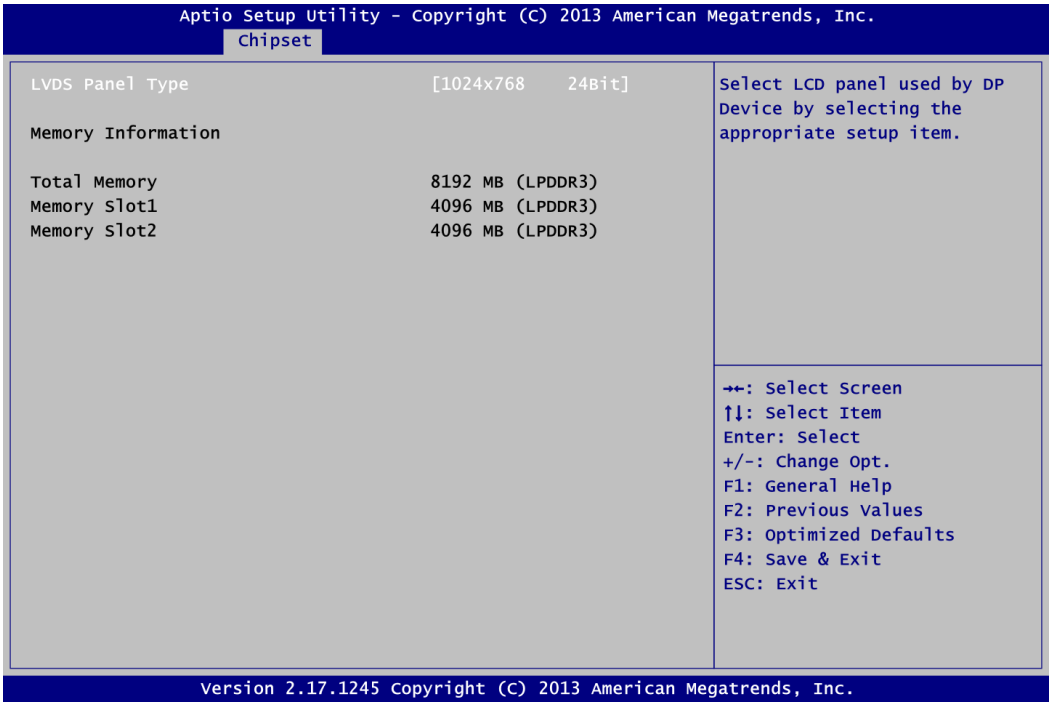
- ► North Bridge
- ► South Bridge

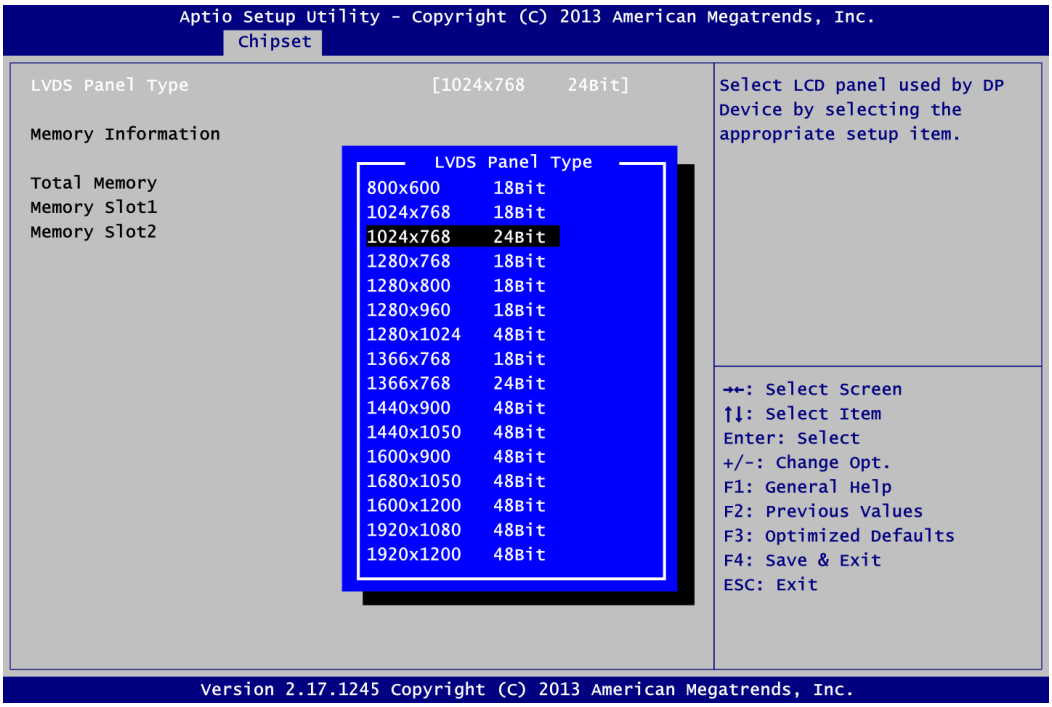
For items marked with "►", please press <Enter> for more options.



North Bridge

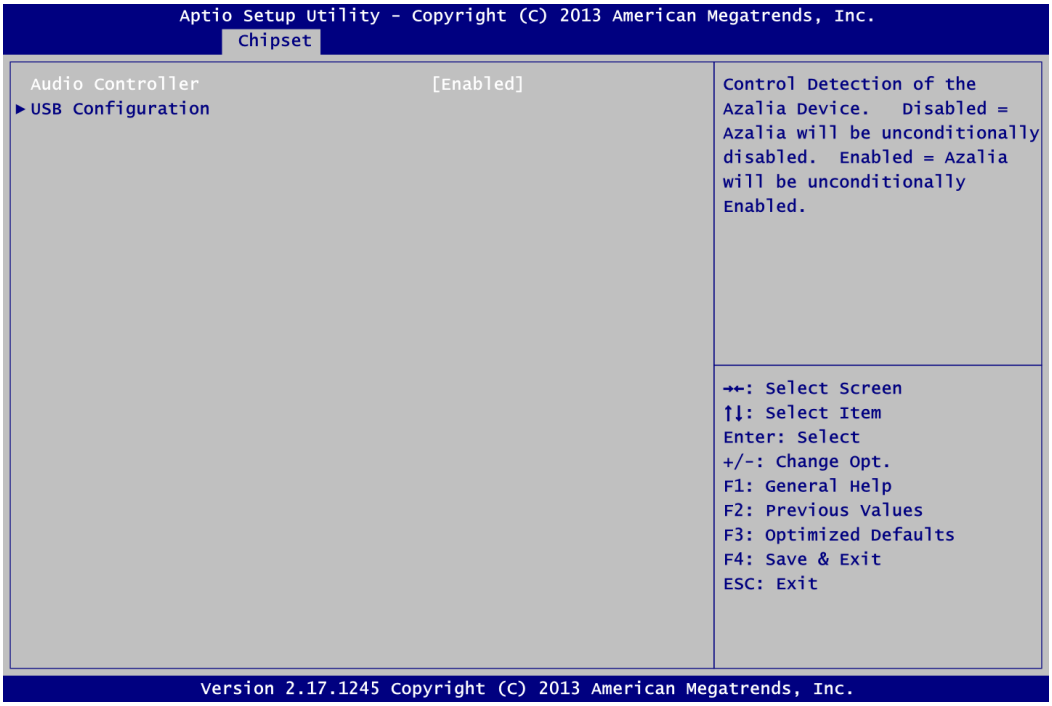
This screen shows system memory information and allows users to configure parameters of North Bridge chipset.



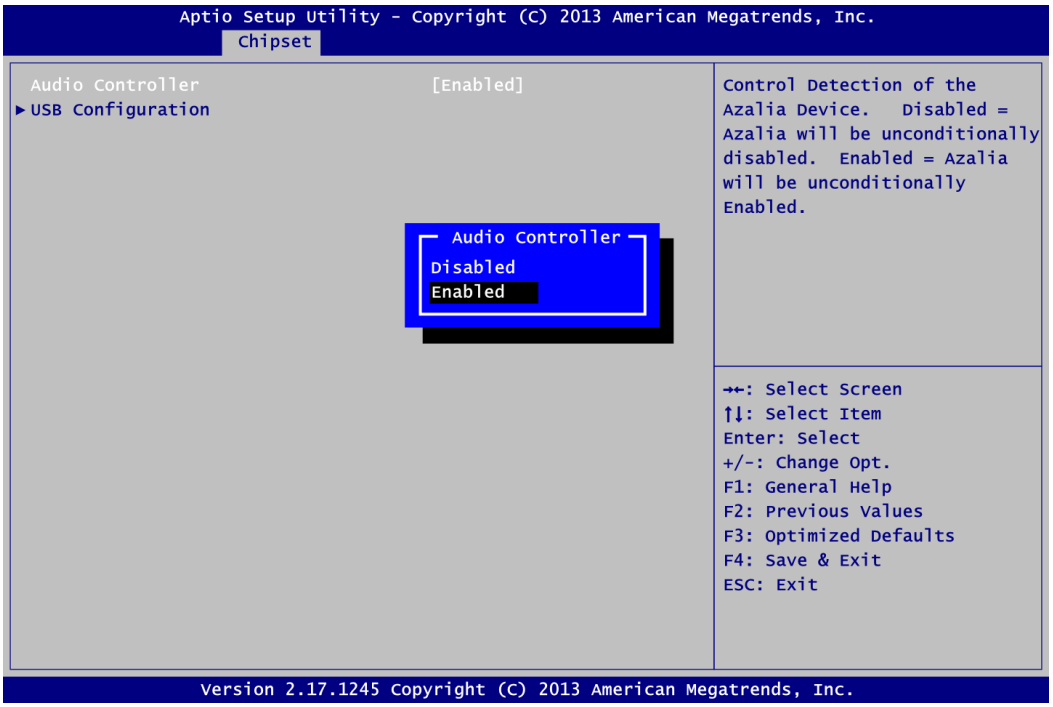


LVDS Panel Type
Select LVDS panel resolution; see the selection options in image above.

- **South Bridge**
  This screen allows users to configure parameters of South Bridge chipset. For items marked with "►", please press <Enter> for more options.

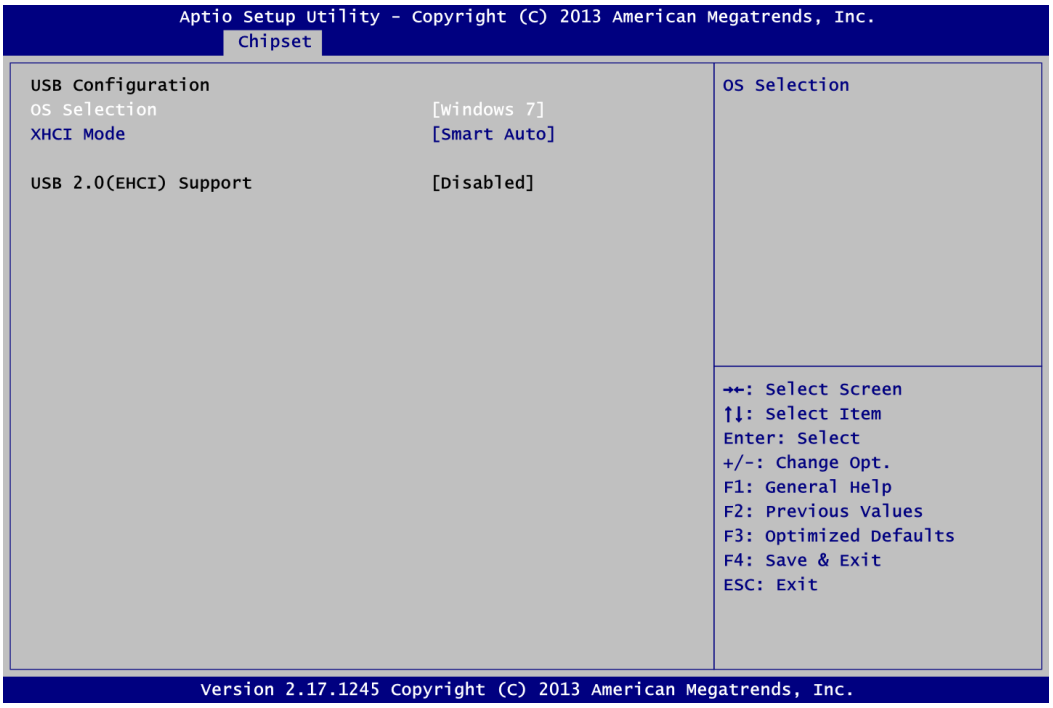


- **South Bridge - Audio Controller**



Audio Controller
Control detection of the HD Audio device.
- Disabled: Audio device will be unconditionally disabled.
- Enabled: Audio device will be unconditionally enabled.

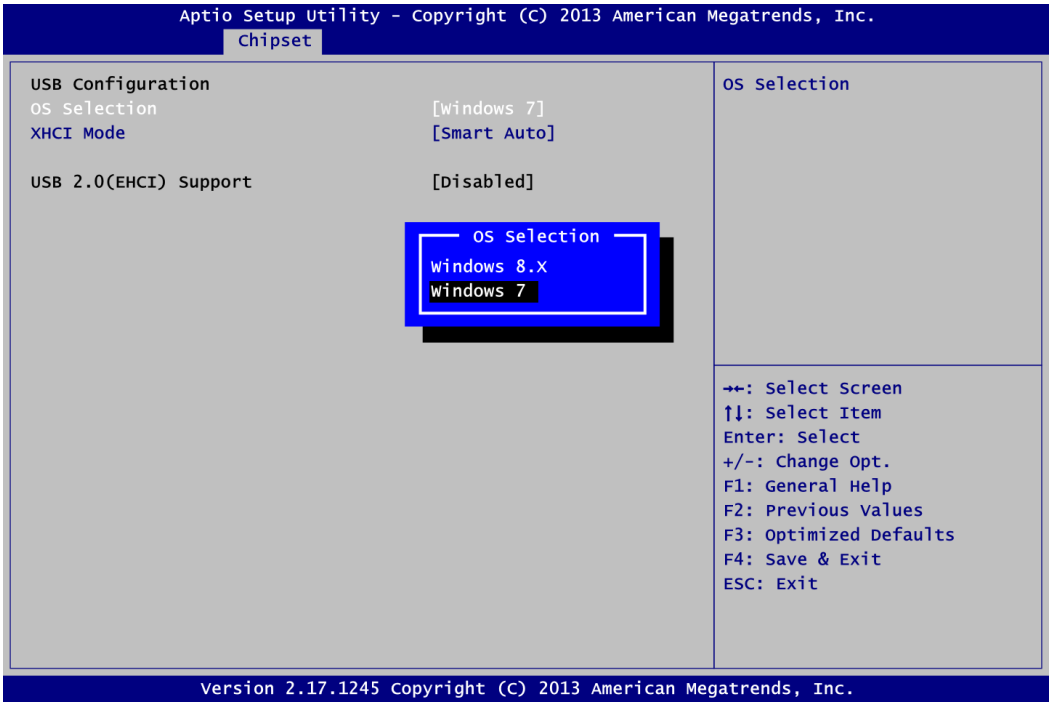
- **South Bridge – USB Configuration**



OS Selection
Use this item to select Windows® 8.x or Windows® 7 operating system to control XHCI Mode default operating mode.

Note

Please use USB 2.0 port 0~3 of COM Express™ connector raw A_B to install Window® 7.



XHCI Mode
Select operation mode of XHCI controller.

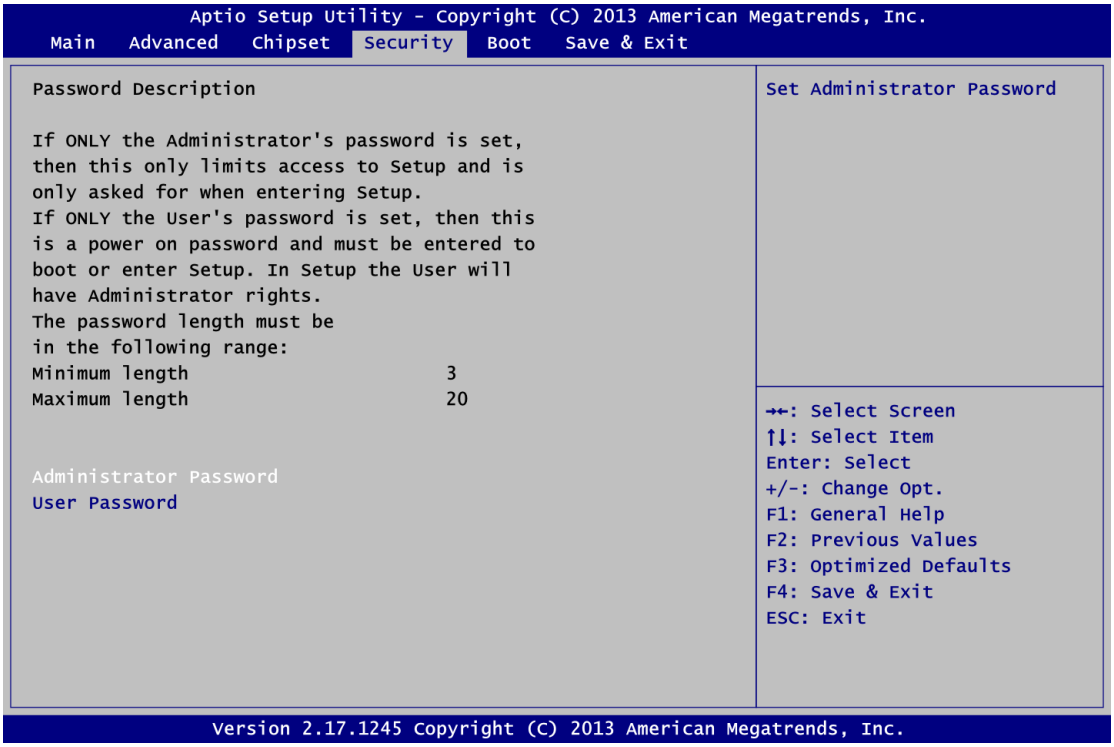
USB 2.0(EHCI) Support
Control the USB 2.0(EHCI) functions. One EHCI controller must always be enabled. This item is selectable if XHCI Mode is Disabled.

Note

In order for the USB 2.0 port 4~7 of COM Express™ connector raw A_B to function properly in Windows® 7, please install USB 3.0 driver in advance.

4.6 Security Menu

The Security menu allows users to change the security settings for the system.

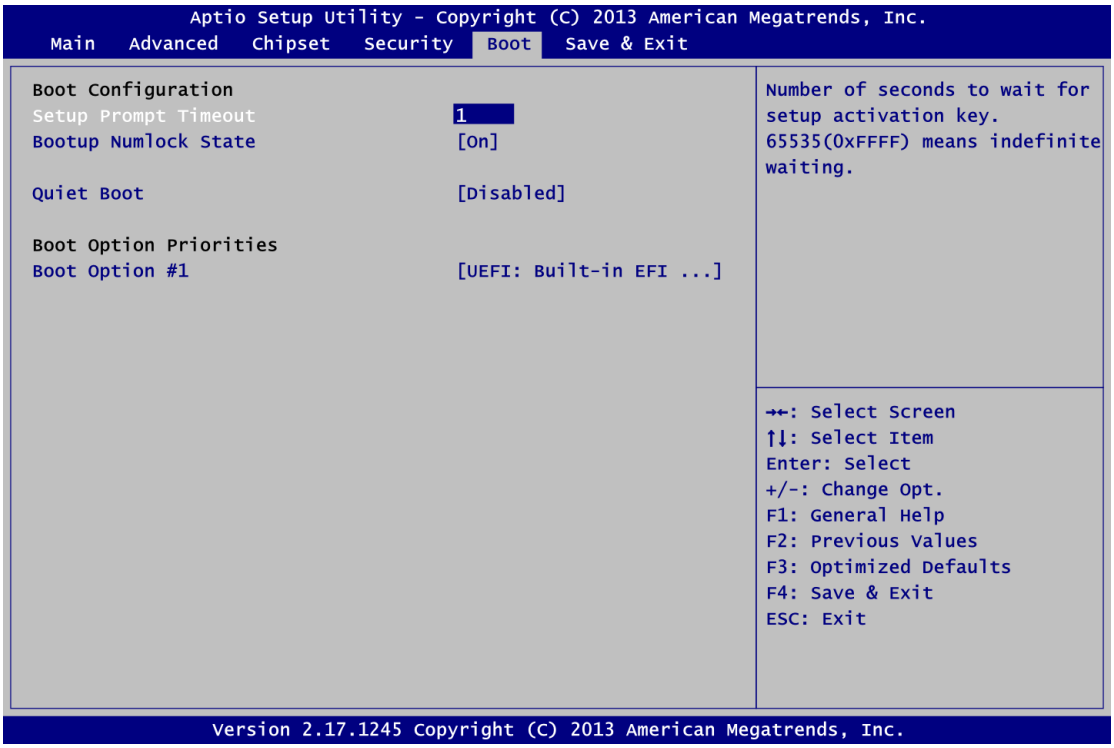


- **Administrator Password**
  Set administrator password.

- **User Password**
  Set user password.

4.7 Boot Menu

The Boot menu allows users to change boot options of the system.



- **Setup Prompt Timeout**
  Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

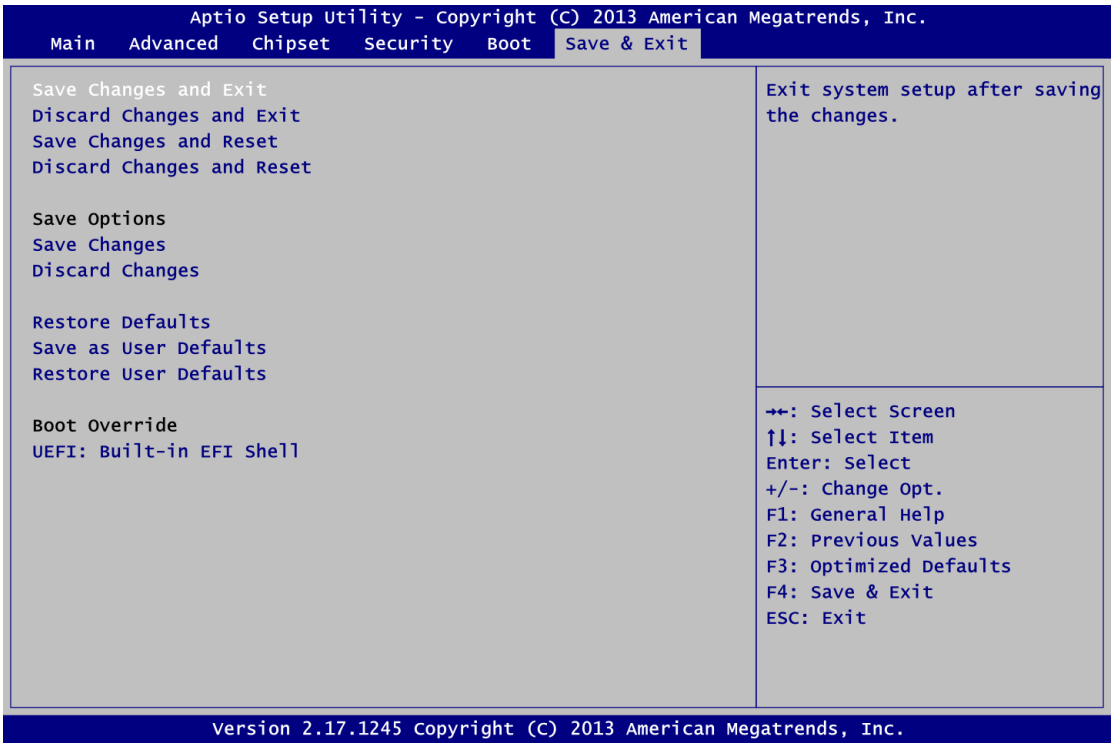
- **Bootup NumLock State**
  Use this item to select the power-on state for the keyboard NumLock.

- **Quiet Boot**
  Select to display either POST output messages or a splash screen during boot up.

- **Boot Option Priorities [Boot Option #1, …]**
  These are settings for boot priority. Specify the boot device priority sequence from the available devices.

4.8 Save & Exit Menu

The Save & Exit menu allows users to load your system configuration with optimal or fail-safe default values.



- **Save Changes and Exit**
  When you have completed the system configuration changes, select this option to leave Setup and continue to boot to operating system. Select Save Changes and Exit from the Save & Exit menu and press <Enter>. Select Yes to save changes and exit.

- **Discard Changes and Exit**
  Select this option to quit Setup without making any permanent changes to the system configuration and continue to boot to operating system. Select Discard Changes and Exit from the Save & Exit menu and press <Enter>. Select Yes to discard changes and exit.

- **Save Changes and Reset**
  When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select Save Changes and Reset from the Save & Exit menu and press <Enter>. Select Yes to save changes and reset.

- **Discard Changes and Reset**
  Select this option to quit Setup without making any permanent changes to the system configuration and reboot the computer. Select Discard Changes and Reset from the Save & Exit menu and press <Enter>. Select Yes to discard changes and reset.

- **Save Changes**
  When you have completed the system configuration changes, select this option to save changes. Select Save Changes from the Save & Exit menu and press <Enter>. Select Yes to save changes.

- **Discard Changes**
  Select this option to quit Setup without making any permanent changes to the system configuration. Select Discard Changes from the Save & Exit menu and press <Enter>. Select Yes to discard changes.

- **Restore Defaults**
  It automatically sets all Setup options to a complete set of default settings when you select this option. Select Restore Defaults from the Save & Exit menu and press <Enter>.

- **Save as User Defaults**
  Select this option to save system configuration changes done so far as User Defaults. Select Save as User Defaults from the Save & Exit menu and press <Enter>.

- **Restore User Defaults**
  It automatically sets all Setup options to a complete set of User Defaults when you select this option. Select Restore User Defaults from the Save & Exit menu and press <Enter>.

- **Boot Override**
  Select a drive to immediately boot that device regardless of the current boot order.

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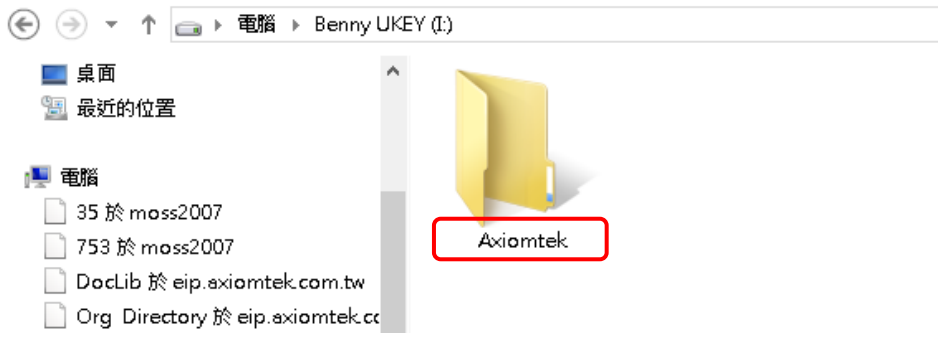
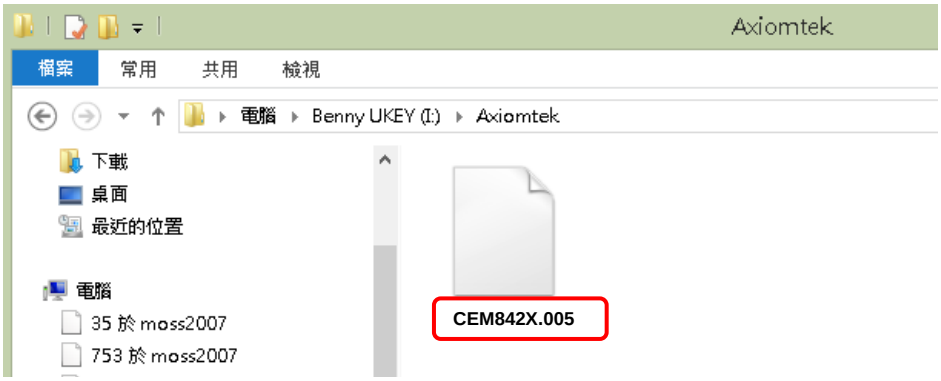
Appendix A
BIOS Flash Utility

The BIOS Flash utility is a new function in BIOS setup program. In this appendix you may learn how to configure it. Please follow instructions below to update system BIOS from BIOS setup menu.

1. In your USB thumb drive, create a new folder and name it “Axiomtek”, see figure below.



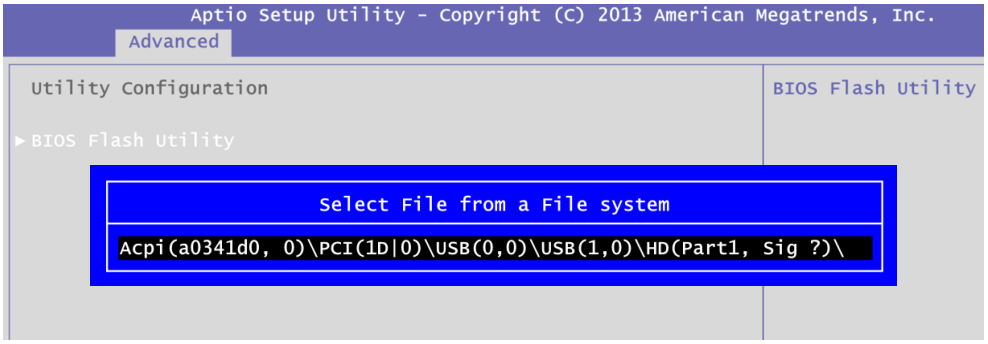
2. Copy BIOS ROM file (e.g. CEM842X.005) to “Axiomtek” folder.



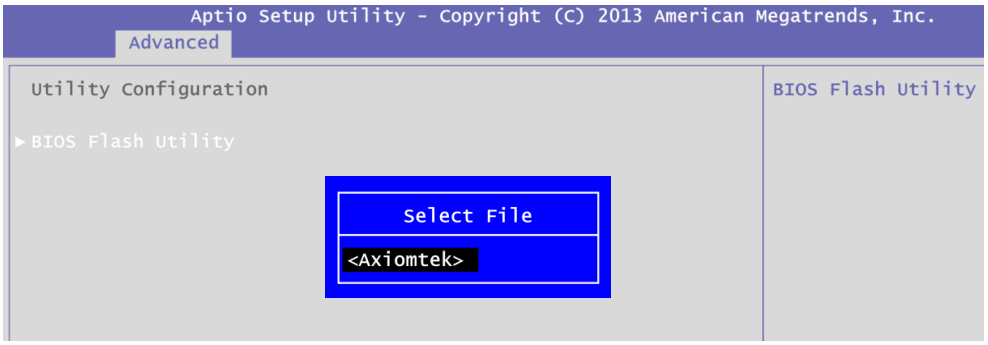
3. Insert the USB thumb drive to your system.

4. Enter BIOS setup menu and go to Advanced\Utility Configuration. Select BIOS Flash Utility and press <Enter>.

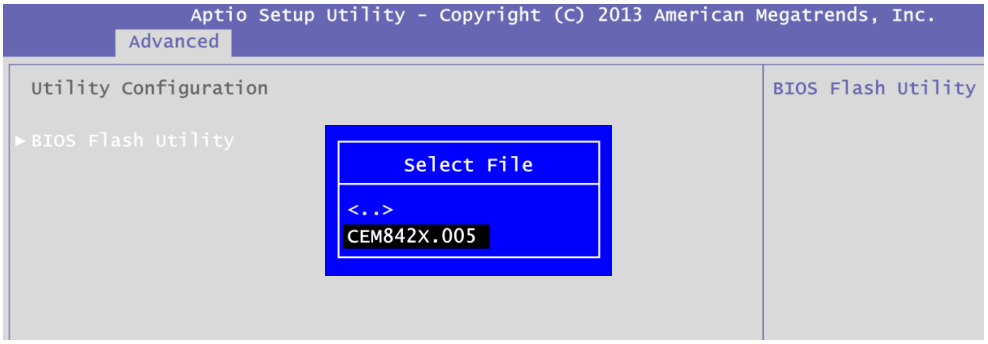
5. BIOS automatically detect all USB drive(s) attached to the system. In this example only one USB drive is attached to the system. That's why, you can see only one device is displayed in figure below.



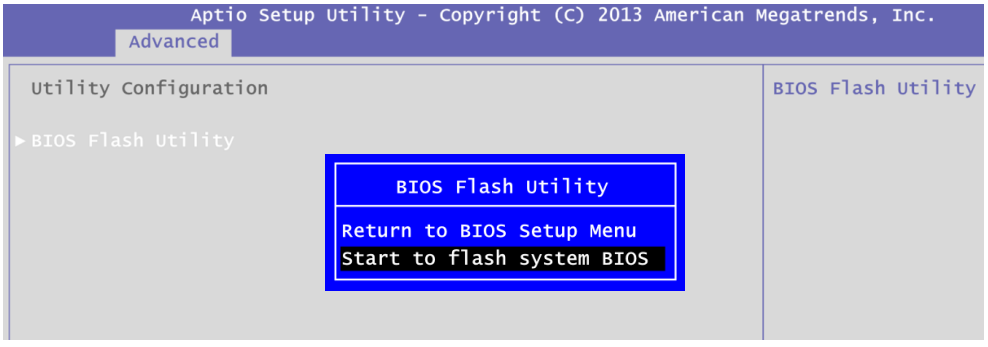
6. Select the USB drive containing BIOS ROM file you want to update using the <↑> or <↓> key. Then press <Enter> to get into "Axiomtek" folder.



7. Now you can see the BIOS ROM file on the screen, press <Enter> to select.

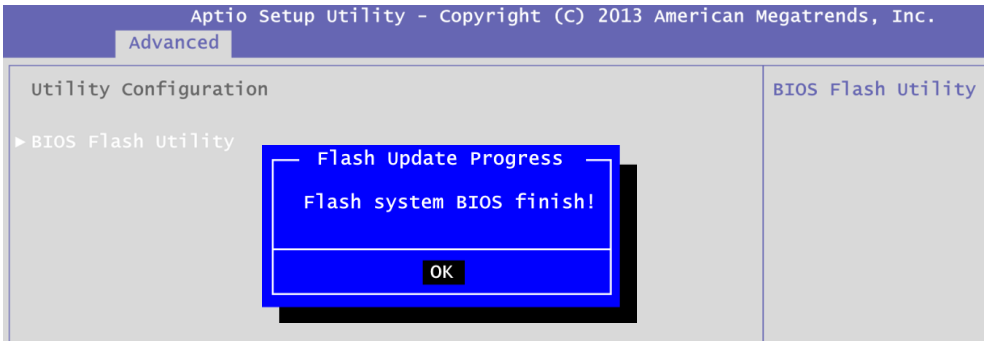


8. Select Start to flash system BIOS option to begin updating procedure.



9. Please wait while BIOS completes the entire flash update process: erase data, write new data and verify data.

10. When you see the following figure, press <Enter> to finish the update process. After that the system will shut down and restart immediately.



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Appendix B
Watchdog Timer and GPIO

B.1 About Watchdog Timer

Software stability is major issue in most application. Some embedded systems are not watched by human for 24 hours. It is usually too slow to wait for someone to reboot when computer hangs. The systems need to be able to reset automatically when things go wrong. The watchdog timer gives us solution.

The watchdog timer is a counter that triggers a system reset when it counts down to zero from a preset value. The software starts counter with an initial value and must reset it periodically. If the counter ever reaches zero which means the software has crashed, the system will reboot.

B.2 About GPIO

The onboard GPIO (general input and output) has 8 bits (GPI0~3 and GPO0~3). In default, all pins are pulled high with +3.3V level (according to main power). The BIOS default settings are 4 inputs and 4 outputs where all of these pins are set to 1. Use these GPIO signals to control cash drawers and sense warning signals from an Uninterrupted Power System (UPS), or perform store security control.

B.2 Sample Program

Programming sample code (from CEM842/843 FINTEK F75111R):

```
/*---------------- INCLUDE FILE ----------------------*/
#include <stdio.h>
#include <conio.h>
#include <bios.h>

#define UCHAR   unsigned char
#define UINT    unsigned int
#define SMIOBASE      0xF040
/******************
       SMIOBASE can get from PCI device Bus-0,Device-31, Function-3
       Register 20h~23h, the value is the IO base address.
*******************/
#define SM_REG         (SMIOBASE+3)
#define SM_ADDR        (SMIOBASE+4)
#define SM_DATA        (SMIOBASE+5)
#define SM_CMD         (SMIOBASE+2)
#define SM_STATUS      (SMIOBASE+0)
#define SM_byteAccess 0x48
#define Device_Addr    0x6E  // depend on hardware designed Low:0x9C, High:0x6E
UCHAR _read_smbus(UCHAR ,UCHAR);
void _write_smbus(UCHAR,UCHAR, UCHAR);
#define F75111_CHIPID           0x0003
#define F75111_VENDORID         0x3419
#define WDTOUT10_CntlReg1       0x34
#define WDTOUT10_2S_bit         0x04    //bit 2
#define WDTOUT10_OINV_bit       0x02    //bit 1
#define WDTOUT10_Status_bit     0x01    //bit 0 , write 1 for clear status
#define WDTOUT10_CntlReg2       0x35
#define WDTOUT10_Enable_bit     0x80    //bit 7
#define WDTOUT10_PTIME          0x7f    //bit 0~6
```

```
/* ------------------ MAIN PROGRAM -------------------*/
main()
{
UCHAR   xch,xch2;
UINT    chipid=0, vendorid=0;
       //Check the Chip ID information
       xch=_read_smbus(Device_Addr,0x5a);     //Chip ID 1
       xch2=_read_smbus(Device_Addr,0x5b);    //Chip ID 2
       chipid=((UINT)xch2 << 8) + (UINT)xch;
       xch=_read_smbus(Device_Addr,0x5d);     //Vendor ID 1
       xch2=_read_smbus(Device_Addr,0x5E);    //Vendor ID 2
       vendorid=((UINT)xch2 << 8) + (UINT)xch;
       if (F75111_CHIPID != chipid || F75111_VENDORID != vendorid )
         { printf("!!! Not found F75111 chip !!!\n");
           exit(-1);
         }
       printf("=== Found F75111 chip ===\n");
       printf("=== GPIO Output Test ===\n");

       //set GPIO3x  direction
       printf("Set F75111 GPIO3x pin is output direction\n");
       _write_smbus(Device_Addr,0x40,0x0f);   //GPIO3x Output direction

       //set GPIO3x output level or plus
       printf("Set F75111 GPIO3x pin is output Level\n");
       _write_smbus(Device_Addr,0x43,0);      //GPIO3x Level control

       //write GPIO3x data
       printf("Write GPIO3x data is 0x0A\n");
       printf("GPO0=0, GPO1=1, GPO2=0, GPO3=1\n");
       _write_smbus(Device_Addr,0x41,0x0a);
       printf("Please check the GPO level and hit any key to continue\n");
       getch();

       //write GPIO3x data
       printf("Write GPIO3x data is 0x05\n");
       printf("GPO0=1, GPO1=0, GPO2=1, GPO3=0\n");
       _write_smbus(Device_Addr,0x41,0x05);
       printf("Please check the GPO level and hit any key to continue\n");
       getch();


       //set GPIO10,11,12 used
       printf("=== GPIO Input Test ===\n");
       printf("Set F75111 GPIO1x is used GPIO function\n");
       xch=_read_smbus(Device_Addr,0x03);
       xch &= 0xE0 ;
       _write_smbus(Device_Addr,0x03,xch);    //set Pin GPIO10/11/12 used
       _write_smbus(Device_Addr,0x04,0);      //set Pin GPIO1x used

       printf("Set F75111 GPIO10,11,12,13 is input function\n");
       _write_smbus(Device_Addr,0x10,0x00);   //set GPIO1x input direction

       printf("Set F75111 GPIO10,11,12,13 is Level mode\n");
       _write_smbus(Device_Addr,0x13,0x00);   //set GPIO1x Level Control

       xch=_read_smbus(Device_Addr,0x12);     //read GPIO1x Status
       printf("Read the GPI0,1,2,3 input data is %02X\n",xch);
       printf("Please Change the GPIx input and hit any key to continue\n");
       getch();
       xch=_read_smbus(Device_Addr,0x12);     //read GPIO1x Status
       printf("Read the GPI0,1,2,3 input data is %02X\n",xch);
       printf("Please Change the GPIx input and hit any key to continue\n");
       getch();
       xch=_read_smbus(Device_Addr,0x12);     //read GPIO1x Status
       printf("Read the GPI0,1,2,3 input data is %02X\n",xch);
       /*****************************************/
       printf("===== WatchDogTimer Test =====\n");
       printf("Set WDTOUT10 pin used\n");
       _write_smbus(Device_Addr,0x01,0x20);   //Pin1 config

       printf("Set WDTOUT10 output 100ms plus, normal level\n");
       _write_smbus(Device_Addr,WDTOUT10_CntlReg1,0);      //WDT10 control

       printf("Set WDTOUT10 Time 10 seconds and enable WDT\n");
       _write_smbus(Device_Addr,WDTOUT10_CntlReg2,0x8A);   //WDT10 control
```

```
        printf("Please hit any key in period of 10 seconds\n");
        getch();
        _write_smbus(Device_Addr,WDTOUT10_CntlReg2,0x8A);   //WDT10 control
        printf("The sytsem will reset when the 10 seconds times out\n");
}

void _write_smbus(UCHAR xAddr,UCHAR xReg, UCHAR xData)
{
        while (1)
        { if (_check_smbus_busy()==0) break;
        }
        outp(SM_REG, xReg);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_ADDR, xAddr);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_DATA, xData);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_CMD, SM_byteAccess);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_STATUS, 02); //clear interrupt status
}

UCHAR _read_smbus(UCHAR xAddr,UCHAR xReg)
{
UCHAR   xch,xch2;
        while (1)
        { if (_check_smbus_busy()==0) break;
        }
        outp(SM_REG, xReg);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_ADDR, xAddr+1);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_CMD, SM_byteAccess);
        xdelay();             //because the CPU too fast,delay for IO
        while (1)
        { if (_check_smbus_busy()==0) break;
        }
        xch=inp(SM_DATA);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_STATUS, 2);  //clear interrupt status
        return xch;
}

_check_smbus_busy(void)
{
UCHAR   xch;
        xch=inp(SM_STATUS);
        if (xch & 0x02 ) outp(SM_STATUS, 2);   //clear interrupt status
        if ( xch & 0x02 ) return 1;
        if ( xch & 0x01 ) return 1;
        return 0;
}

xdelay()
{
int     xxi,xxj,xxk=0;
        for (xxi=0 ; xxi< 0x1000 ; xxi++) {
                for (xxj=0 ; xxj < 0x100 ; xxj++) {
                        xxk++;
                }
        }
}
```